BIPOLAR JUNCTION TRANSISTOR

Introduction:

The transistor was invented by Dr. William Shockley & Dr. John Bardeen at Bell laboratory in America in 1951. First time, in 1952 transistor was used in telephone switching circuits. since, then, it was revolution sized the field of Electronics.

The transistor has replaced the bulky vacuum tubes in most of the electronic circuits. The transistor is a basic building block of all model electronic systems. It is a three terminal device. The output voltage, current or power are controlled by the input current in a transistor. Therefore, it is called a current-controlled device.

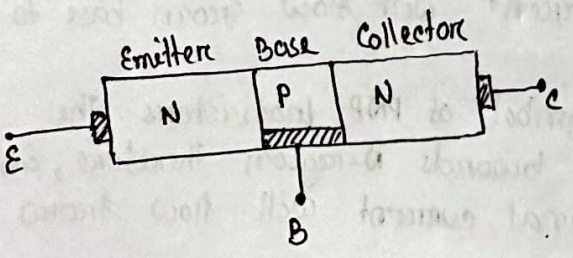
BJT stands for Bipolar Junction Transistor because the transistor operation is carried out by two types of charge carriers; majority & minority carriers. A transistor has a very important property that it can raise the strength of an input weak signal. This property is called Amplification. Due to this quality, the transistor is one of the most widely used semiconductor devices.

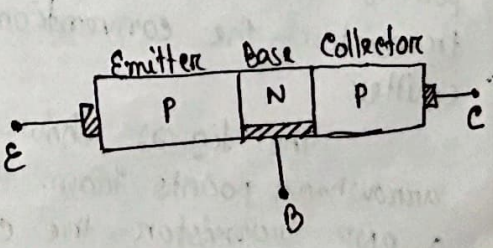
Applications:

→ Transistor is used in control system.
→ Transistor is used in satellites & mobile phones.
→ In digital computer electronics, the transistor is used as a high speed electronic switch.
→ In communication systems, it is widely used as the primary component in the amplifier.

Junction Transistor Construction:

A transistor is a single crystal of silicon (Si) or Germanium (Ge). A transistor can be of two types: NPN or PNP. A transistor consists of two pn-junctions. The junctions are formed by sandwiching either p-type or n-type semiconductor layers between a pair of opposite types as shown in fig.





A transistor has three regions. They are emitter, base & collector.

→ Emitter: It is an outer region situated in one side of transistor. The function of emitter is to inject charge carriers (electrons in case of NPN & holes in case of PNP transistors) into base. Since emitter has to supply a large no. of charge carriers, so it is heavily doped More is the doping more will be the available charge carriers.

→ Base: It is the middle region of the transistor. The base is very thin & lightly doped region. The function of this region is to pass all the charge carriers (electrons or holes) onto the collector.

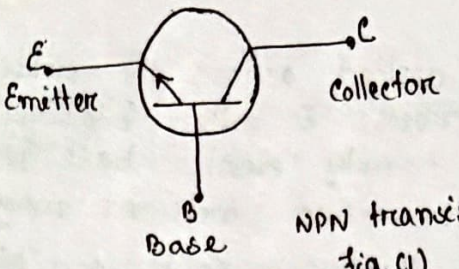
→ Collector: It is the other outer region situated in the other side of transistor. The doping of collector is between the heavy doping of emitter & light doping of Base. The function of collector is to collect charge carriers (electrons or holes). The collector region is physically larger than the emitter region. The reasons for this is that the collector has to dissipate more heat. Hence, it is clear that although a BJT has two same type of outer regions, their functions can not be interchanged.

A transistor has two PN-junctions. One junction is formed between the emitter & the base is called emitter-base region or junction. And the junction is formed between base & the collector is called collector-base junction.

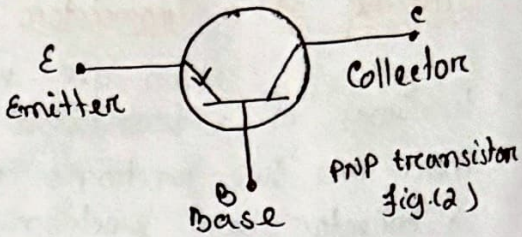
Transistor Symbols:

There are two types of transistor is known as NPN or PNP. The fig.(1) represents the symbol of NPN transistors. The emitter has an arrowhead. The arrowhead indicates the direction of conventional current flow in a transistor. The arrowhead points from p-region towards the N-region. Therefore, in a NPN transistor the conventional current will flow from base to emitter.

The fig.(2) shows the symbol of PNP transistors. The arrowhead points from p-region towards N-region. Therefore, in a PNP transistor the conventional current will flow from emitter to base.



NPN transistor
fig. (1)



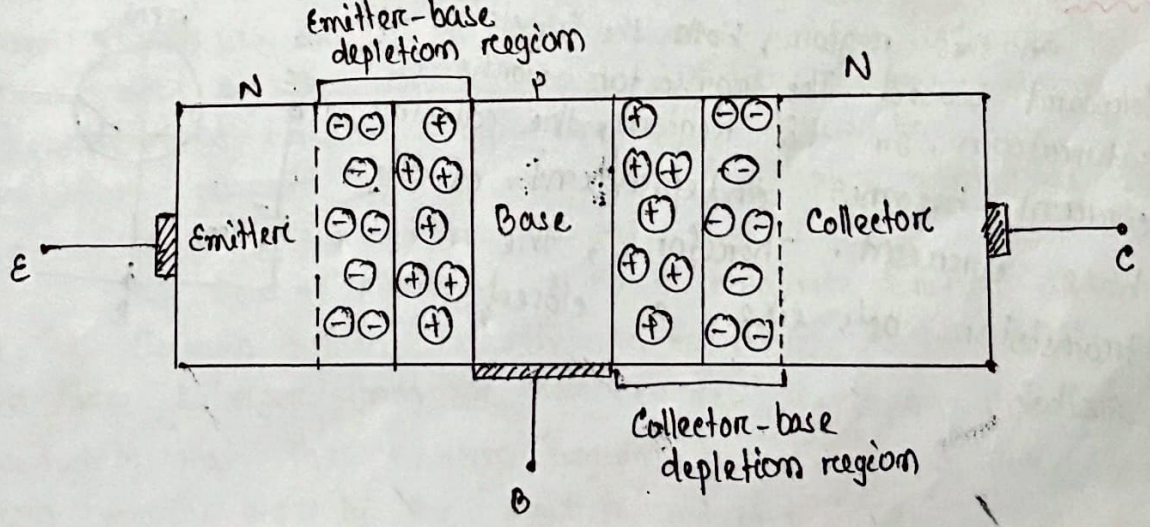
PNP transistor
fig. (2)

The PNP transistor is a complement of the NPN transistor. Hence, in a NPN transistor, the majority carriers are free electrons but in PNP transistor majority carriers are holes. The currents & voltages involved in the action of PNP transistor are opposite to those of NPN transistor.

Out of these two types of transistors, the NPN transistor is mostly used. The reason for this is that of NPN transistors, the current conduction is mainly by electrons where as in PNP transistors the current conduction is mainly by holes. since electrons are more mobile than holes, the conduction is higher in NPN transistors than PNP transistors.

Unbiased Transistor :

When no battery is connected between the different terminal of a transistor then the transistor is said to be unbiased state or open circuit state. on this condition, the diffusion of charge carriers across the junction produces two depletion regions. The barrier potential for each of these two depletion layer is 0.7V for Si & 0.3 for Ge. But the three regions have different doping levels, so the depletion width are not the same for two junctions. Since emitter is heavily doped than base & collector, the emitter-base depletion region width is smaller than that of collector-base depletion region width.



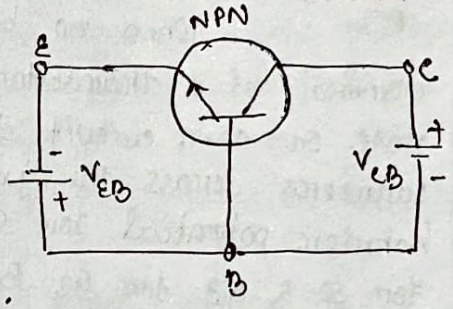
Biasing of a Transistor :

When d.c. voltages are applied across the different terminal of a transistor, then this process is called biasing. Since, there are two junctions in transistor namely emitter-base junction & collector-base junction, each of these two junctions may be forward-biased or reverse-biased. There are four possible ways of biasing these two junctions. These possible ways are called modes of operation of transistor.

Cases	Emitter-Base Junction	Collector-Base Junction	Region of Operation
1	Forward-biased	Reverse-biased	Active
2	Forward-biased	Forward-biased	Saturation
3	Reverse-biased	Reverse-biased	Cut-off
4	Reverse-biased	Forward-biased	Inverted

Case-1 (Active Region) :

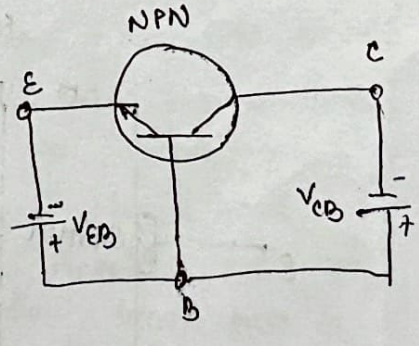
In this mode, the emitter-base junction is forward-biased & collector-base junction is reverse-biased.



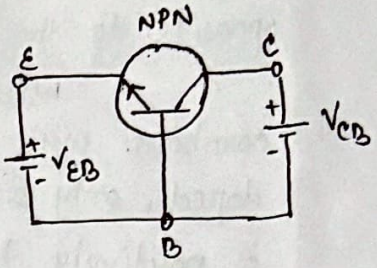
The battery V_{EB} is connected between emitter & base, so as to make emitter-base junction forward-biased. Similarly, battery V_{CB} makes collector-base junction reverse-biased. In this region, transistor used for amplification. In this region, the collector current depends upon the base current.

Case-2 (Saturation Region) :

In this region, both the junctions are forward biased. The transistor works in saturation. In this region, the collector current becomes independent of the base current. Therefore, the transistor acts like a closed switch.

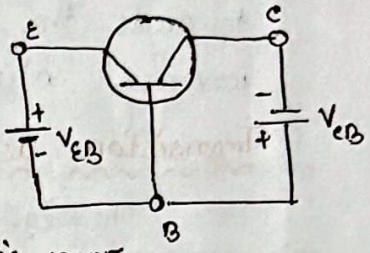


Case-3 (Cut-off Region):



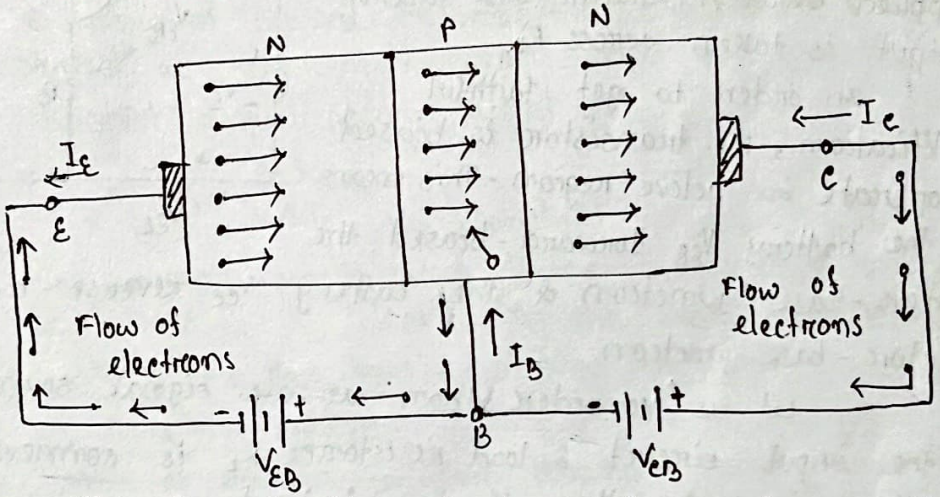
On this mode, both the junctions are reverse biased. On this region, the transistor has practically zero current because the emitter does not ~~exist~~ emit charge carriers into the base & no charge carriers collected by the collector except a few thermally generated minority carriers. The transistor is open in this mode when it is used as an open switch.

Case-4 (Inverted Region):



In this condition, the emitter-base region is reverse-biased & collector-base junction is forward-biased. Since, the doping level of emitter & collector is not same, therefore, the collector can not inject the majority charge carriers into the base. In this region, the action of transistor is poor.

Working of a Transistor:



The emitter-base junction is forward biased by battery V_{EB} & collector-base junction is reversed biased by battery V_{CB}. The forward-biased voltage is small & reversed-biased voltage is quite large. The forward bias on the emitter-base junction pushes a large number of free electrons in the N-type emitter towards the base. This makes the emitter current (I_E). A very ~~few~~ few holes also pass from the base region to the emitter region.

This flow of electrons & holes constitute emitter current (I_E). Since, the electron current is useful in the action of transistor, it is made larger & larger than the hole current by doping the base region more lightly than the emitter region. Hence, only a very small portion nearly 0.5% of the emitter current is due to the holes passing from base to emitter.

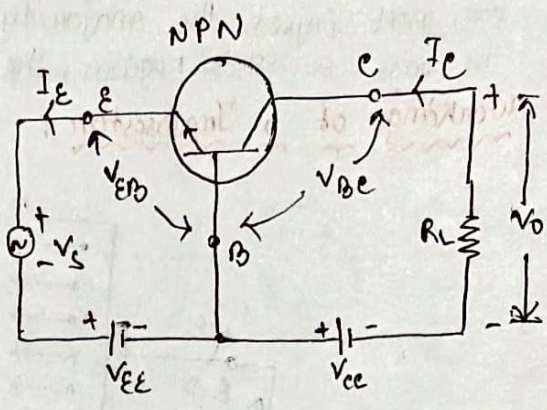
The direction of conventional current is always taken opposite to the flow of electrons.

After reaching the base region, the electron tend to combine with holes. But since the base is very thin & lightly doped, only a very few electrons pass on the collector which is positively biased N-region. These electrons collected by the collector to constitute the collector current.

There is one another component of collector current due to thermally generated. Minority carriers (holes) which pass towards the base. This small current component is called reverse saturation current.

Transistor as an Amplifier :

The fig. shows the common-base NPN transistor. The emitter is input terminal & the collector is output terminal. The weak input signal is applied between emitter-base junction & output is taken across R_L.



In order to get faithful amplification, the transistor is biased to operate in active region. This means that the battery V_{EE} forward-biased the emitter-base junction & the battery V_{cc} reverse-biased the collector-base junction.

Let us consider, than an a.c. signal source V_s is connected in the input circuit & load resistance R_L is connected in output circuit. An output voltage V_o is obtained across resistance R_L. When the input signal V_s is superimposed on the d.c. voltage V_{EE}, the emitter-base voltage V_{EB} varies with time. Due to this, the emitter current I_E also varies. We know the collector current is a function of emitter current, therefore similar variations occur in the collector current. This varying current pass through the load (R_L) & so a varying voltage V_o. The output voltage V_o will be greater than the input signal V_s.

* An Amplifier is a circuit which magnifies or increases the amplitude of a signal waveform applied to it. However, it may be note that only amplitude is changed & shape of waveform remains unchanged.

Module - II

Field Effect Transistor:

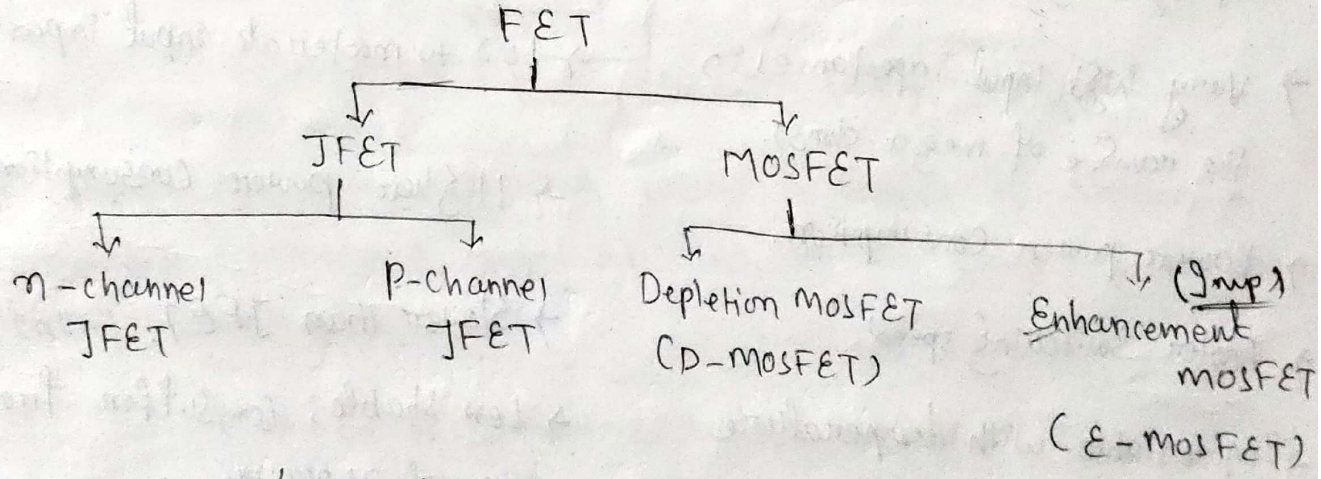
The field effect transistor appriviated as FET is an another Semiconductor device like a BJT which can be used as an amplifier or as a switch.

→ Like BJT, FET is also a three terminal device, however the principle of operation of FET is completely different from the BJT.

→ The name field effect is derieved from the fact that the flow of current through the conducting region is controlled by an electric field.

Types of FET:

Base on the construction the FET can be classified in to two type one is Junction Field Effect Transistor (JFET) & another one is Metal oxide Semiconductor field effect transistor (MOSFET).



FET is a voltage control device. Becuz output current is control by varying the input voltage.

FET is a unipolar device becuz the current conduction is only by majority charge carriers.

The three terminal of FET are named as:-

(a) Drain (D)

(b) Source (S)

(c) Gate (G)

Out of these terminal Gate terminal act as a controlling element.

* Difference between JFET & BJT.

Ans:

JFET	BJT
→ This is Unipolar (uses only majority carriers)	→ This is Bipolar (uses both majority & minority carriers)
→ Uses only electrons (N-channel) or holes (p-channel).	→ Uses both e^- & holes.
→ Voltage controlled device. (input voltage controls output current)	→ Current controlled device, (input current controls output current)
→ Very high input impedance (in the range of mega-ohms).	→ Low to moderate input impedance
→ Lower power consumption.	→ Higher power consumption.
→ Faster switching speed	→ Slower than JFET.
→ More stable with temperature variations	→ Less stable; can suffer from thermal runaway.
→ Lower gain compared to BJT.	→ Higher current gain.
→ Used in high impedance circuits, amplifiers and RF applications.	→ Used in power amplification, switching and signal processing.

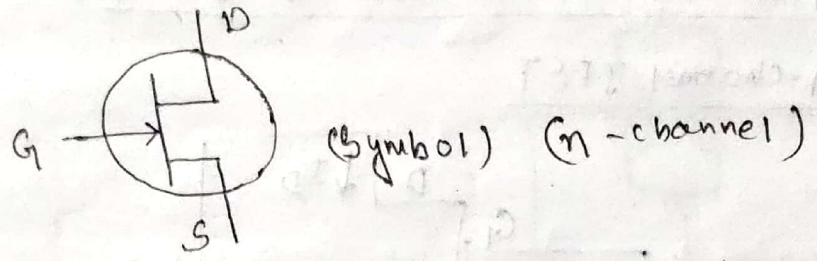
JFET:

Depending upon the majority carrier JFET has been classified in to two types such as:-

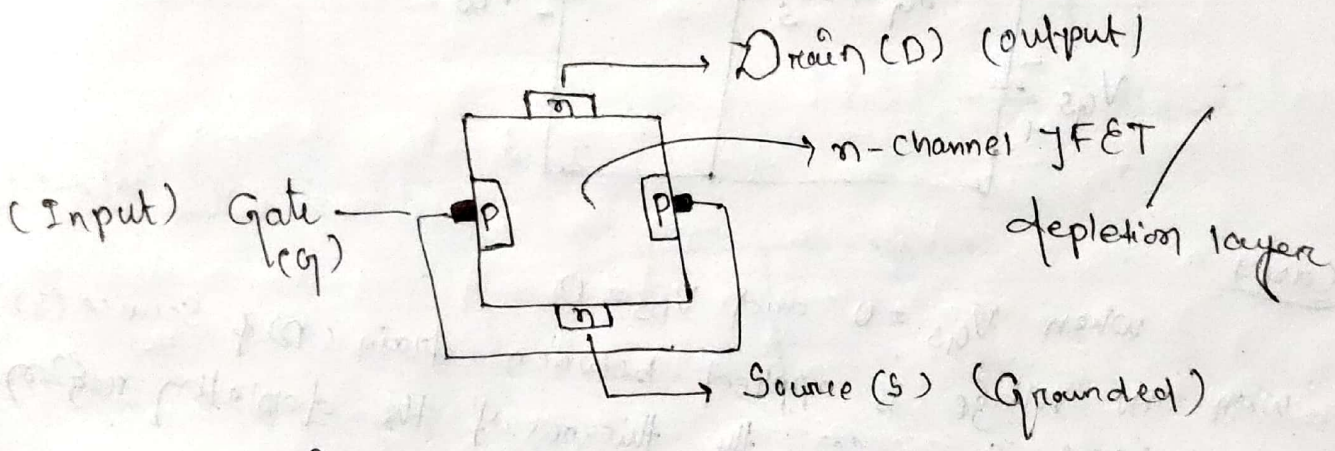
(a) N-channel JFET with e^- as majority carriers.

(b) P-channel JFET with holes as a majority charge carriers.

Construction and Symbol of JFET:



(Symbol) (n-channel)



It consists of a n-type bar which is made of silicon. Ohmic contact (teremnal), made at the two ends of the bar are called Source & drain.

Source: This terminal is connected to the negative terminal of the battery. e^- which are the majority carrieres in the n-type bar.

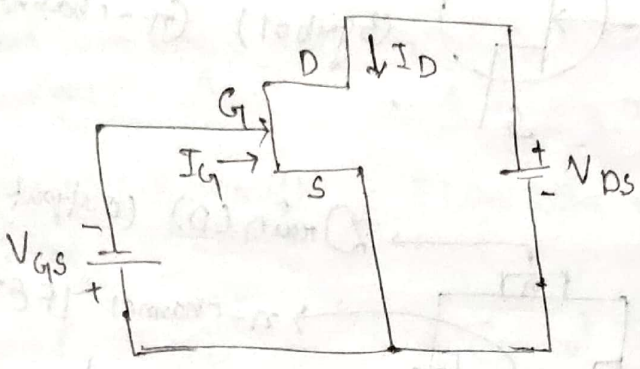
Drain: The terminal is connected to the +ve terminal of the battery. The majority carrier (e^-) leave the bar through this terminal.

Gate: Heavily doped p-type silicon is defused on both sides of the n-type silicon bar by which p-n junction are formed. These layers are joined together called as gate.

Channel: The thin region between the two p-type gates is called the channel. Since, the channel is in the n-type bar the FET is known as n-channel JFET.

Operation / Static characteristic of JFET:

n-channel JFET



Case-1

when $V_{GS} = 0$ and $V_{DS} = 0$

When no voltage is applied between drain (D) & Source (S) and Gate (G) & Source (S) the thickness of the depletion region of the p-n junction is uniform.

Case-2

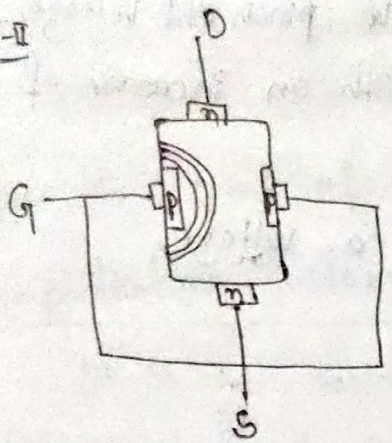
when $V_{DS} = 0$ and V_{GS} = negative

In this case the p-n junction are reverse bias and the thickness of the depletion region increases. As V_{GS} is decrease from 0 the reverse bias voltage across the p-n junction is increased and hence the thickness of the depletion region in the channel until the two depletion region make contact with each other. In this condition the channel is said to be cut-off, the value of V_{GS} which is required to cut-off the channel is called cut-off voltage.

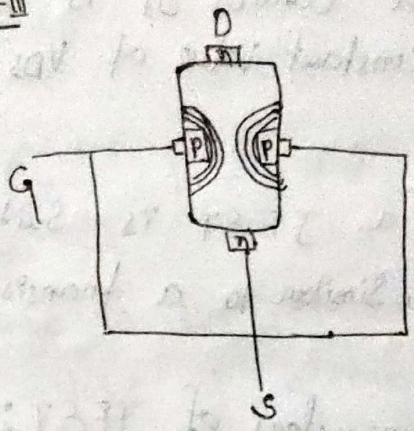
Case-3: when $V_{GS} = 0$ and V_{DS} = positive (Increases) to the Source

Drain is positive with respect to the Source, with $V_{GS} = 0$. Now, the majority carrier i.e e^- flow through the channal from Source to drain. Therefore the Conventional current I_D flows from drain to Source. The magnitude of current will depend upon the many factors. Thus, the channel act as a resistor.

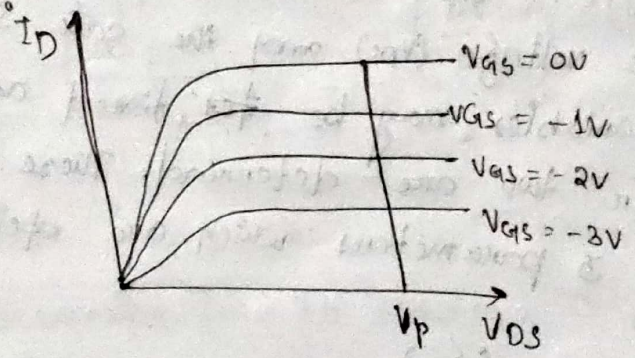
Case-II



Case-III



Characteristics Curve:



As V_{DS} is increased from 0, I_D increase. The region from $V_{DS} = 0$ V to ~~V_{DS}~~ V_{DS} region = V_p (Pinch off voltage) is ohmic region.

when $V_{DS} = V_p$, I_D becomes maximum. when V_{DS} is increased beyond V_p the length of the pinch off region increases. Hence, there is no further of increase in I_D current.

At a certain voltage I_D suddenly increases, this effect is due to the ~~Average~~ avalanche multiplication of e^- caused by breaking of covalent bonds of Si atoms in the depletion region between the Gate (G) and drain (D).

Case-4: When V_{GS} = negative & V_{DS} = Increased

When the gate is maintain at a negative voltage less than the negative cut off voltage. The reverse voltage across the junction is further increased. Hence for a negative value of V_{GS}, the curve of I_D versues V_{DS} is same same as above characteristics.

* From the curves it is seen that above the pinch off voltage, at a constant value of V_{DS}, I_D increases with an increase of V_{GS}.
* Hence a JFET is suitable for use as a voltage amplifier, similar to a transistor amplifier.

Factors / Parameters of JFET:

In a JFET, the drain current (I_D) depends upon the drain source voltage (V_{DS}) and the gate source voltage (V_{GS}). Any of these variables may be ~~fet~~ fixed and the relationship between the other two are determind. These relation are determined by 3 parameters which are define below :-

(1) Trans Conductance (g_m)

It is the slope of the transper characteristic curve and is defined as

$$g_m = \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$$

$$= \frac{\Delta I_D}{\Delta V_{GS}}$$

It is the ratio of a small change in the drain current to the corresponding small change in Gate voltage at a constant drain voltage.

→ g_f has the unit of conductance in mho (℧).

(2) Drain Resistance (r_d)

g_f is the reciprocal of the slope of the drain characteristic is defined as :-

$$r_d = \left(\frac{\partial V_{DS}}{\partial I_D}\right)_{V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D}$$

g_f is the ratio of small change in drain voltage to the corresponding small change in drain current at a constant gate voltage.

→ g_f has the unit of ohm (Ω).

(3) Amplification factor (μ)

g_f is the ratio of a small change in the drain voltage to corresponding small change in gate voltage at a constant drain current.

$$\mu = -\left(\frac{\partial V_{DS}}{\partial V_{GS}}\right)_{I_D} = -\left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right)$$

Here the negative sign shows that when the V_{GS} increased V_{DS} decreased for I_D remains constant.

* Relationship among FET parameters :

As I_D depends on V_{DS} & V_{GS} the functional Equation can be represented as :-

$$I_D = f(V_{DS}, V_{GS})$$

If the drain voltage change by a small amount from V_{DS} to $V_{DS} + \Delta V_{DS}$, the gate voltage change by a small amount from V_{GS} to $V_{GS} + \Delta V_{GS}$ then the corresponding small change in I_D may be obtained by applying

Taylor's theorem with neglecting higher order terms. Thus the small change in ΔI_D is given by :-

$$\Delta I_D = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \Delta V_{DS} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} \Delta V_{GS}$$

Dividing ΔV_{GS} on both sides :-

$$\frac{\Delta I_D}{\Delta V_{GS}} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \frac{\Delta V_{DS}}{\Delta V_{GS}} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} \frac{\Delta V_{GS}}{\Delta V_{GS}}$$

$$\Rightarrow \frac{\Delta I_D}{\Delta V_{GS}} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \frac{\Delta V_{DS}}{\Delta V_{GS}} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$$

$\Rightarrow$ If I_D is constant then

$$\left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \frac{\Delta V_{DS}}{\Delta V_{GS}} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} = 0$$

$$\Rightarrow \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \cdot \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right)_{I_D} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} = 0$$

$$\Rightarrow \frac{1}{r_d} \cdot (-R) + g_m = 0$$

$$\Rightarrow g_m - \frac{R}{r_d} = 0$$

$$\Rightarrow g_m = \frac{R}{r_d}$$

$$\Rightarrow \boxed{R = g_m \cdot r_d}$$

The relationship between these three factors is

$$\boxed{\mu = g_m \cdot r_d}$$

Therefore amplification factor (μ) is the product of drain resistance (r_d) and trans conductance (g_m).

Prob. When a reverse gate voltage of 12 volt is applied to JFET the gate current is 1 nA. Determine the resistance between gate & source.

Ans: Given; $I_D = 1\,nA = (1\times10^{-9})$ amp

$V_G = -12\,V$

r_G = calculated

So, $r_G = \frac{V_G}{I_G}$

$= \frac{-12}{10^{-9}}$

$= -12\times10^{9}\ \Omega$

(Q) When the reverse gate voltage of JFET changes from 4 to 3.9 the drain current changes from 1.3 to 1.6 mA. Find the value of trans conductance.

Ans: Given, $\Delta V_{GS} = 4 - 3.9 = 0.1\,V$

$\Delta I_D = 1.6 - 1.3 = 0.3\,mA$

So, $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$

$= \frac{0.3\times10^{-3}}{0.1}$

$= 0.003\ \mho$

MOSFET

MOSFET is an important Semiconductor device which is widely used in many applications. Like JFET, MOSFET has three terminals i.e Gate, Source & Drain. MOSFET is also called IGFET (Insulated Gate Field Effect Transistor) because the Gate of a MOSFET is insulated from the Channel.

→ MOSFET is classified in to two types:-

(a) Enhancement MOSFET [E-MOSFET]

(b) Depletion MOSFET [D-MOSFET]

Working Principle:

By applying a transverse electric field across an insulator, Deposited on the Semiconducting material - The resistance of the conducting channel of a semiconducting material can be controled.

In a D-MOSFET, the controling electric field reduces the number of majority carriers available for conduction whereas in the E-MOSFET application of electric field causes an increase in the no. of majority carrier in the conducting region of a transistor.

E-MOSFET:

:- DIGITAL ELECTRONICS & CIRCUIT :- __/__/____

Introduction :

→ Digital devices are based on electronic circuitry, which represent two states ON or '1' (high) & OFF or '0' (low) state. Digital circuits are used to store, evaluate & modify digital codes. Integrated circuits have made it possible to design circuits which are capable of handling large quantities of digital encoded data at high speed.

→ The digital word means discrete units like the number of fingers, match sticks etc., which can express as a whole no. & Analog means establishing similarities between two quantities. Digital & Analog are used in control systems, instrumentations, communications, computers & industrial automation. Digital methods of operation offer greater speed precision, accuracy & more reliable & effective than Analog methods. Digital methods are also less affected by noise as compared to analog methods. More over the information can be easily stored in digital systems.

→ **Bit :** Bit is the basic unit of memory & the two binary digits are '0' & '1'. Any binary number can be represented by a string of these two binary digits.

→ **Byte :** Byte is a string of 8-bits such as 10110111, it is the basic unit of binary information & storage. Most computers process data with a length of 8-bits or some multiple of 8-bits.

→ **Nibble :** Nibble is a string of 4-bits such as 1101, 1010 etc. It is half of byte.

→ **Word :** In digital systems a group of bits which is stored, operated & moved around is called a word. One word consists of 16-bits or two bytes. In which first 8-bits represents upper byte & last 8-bits represent lower byte.

→ **Digital System :** In our ordinary system of numbers called arabic numerals. we have 10 symbols 0, 1, ... 9. The digital system has a base of 10.

__/__/____

Number systems :

→ Binary system :

Binary numbers have a base or radix of 2 because only two digits '0' & '1' are used. Any decimal number can be represented in the binary system by a string of 0's & 1's.

Decimal to Binary Conversion :

→ Convert 52_{10} to binary

```
2|52
2|26 → 0 (LSB)
2|13 → 0
2|6  → 1
2|3  → 0
2|1  → 1
  0  → 1 (MSB)
```

So, $(52)_{10} = (110100)_2$

→ Convert 53.625_{10} to binary

```
2|53
2|26 → 1
2|13 → 0
2|6  → 1
2|3  → 0
2|1  → 1
  0  → 1
```

$0.625 \times 2 = 1.25 \rightarrow 1$

$0.25 \times 2 = 0.50 \rightarrow 0$

$0.50 \times 2 = 1.00 \rightarrow 1$

$(0.625)_{10} = (101)_2$

$(53)_{10} = (0110101)_2$

So, $(53.625)_{10} = (110101.101)_2$

Binary to Decimal Conversion :

→ Convert $(11111001001)_2$ to decimal

$(11111001001)_2$

$= 1\times2^{10} + 1\times2^9 + 1\times2^8 + 1\times2^7 + 1\times2^6 + 0\times2^5 + 0\times2^4 + 1\times2^3 + 0\times2^2 + 0\times2^1 + 1\times2^0$

$= 1993$

→ Convert $(11.0111)_2$ to decimal

$(11.0111)_2$

$= 1\times2^1 + 1\times2^0 + 0\times2^{-1} + 1\times2^{-2} + 1\times2^{-3} + 1\times2^{-4}$

$= 2 + 1 + 0 + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} = 3\frac{7}{16}$.

__/__/____

Decimal to Octal Conversion:

→ Convert $(378)_{10}$ to Octal.

8 | 378
8 | 47 → 2
8 | 5 → 7
0 → 5 ↑

So, $(378)_{10} = (572)_8$

→ Convert $(444.456)_{10}$ to Octal

8 | 444
8 | 55 → 4
8 | 6 → 7 ↑
0 → 6

$0.456 \times 8 = 3.648 \rightarrow 3$ ↓
$0.648 \times 8 = 5.184 \rightarrow 5$
$0.184 \times 8 = 1.472 \rightarrow 1$

$(444)_{10} = (674)_8$ $(0.456)_{10} = (351)_8$

So, $(444.456)_{10} = (674.351)_8$

Octal to Decimal Conversion:

→ Convert $(237)_8$ to Decimal

$(237)_8 = 2 \times 8^2 + 3 \times 8^1 + 7 \times 8^0$
$= (159)_{10}$

→ Convert $(120.358)_8$ to decimal

$(120.358)_8 = 1 \times 8^2 + 2 \times 8^1 + 0 \times 8^0 + 3 \times 8^{-1} + 5 \times 8^{-2} + 8 \times 8^{-3}$
$= 80 + \frac{3}{8} + \frac{5}{64} + \frac{8}{512}$
$=$

Octal to Binary conversion:

→ Convert $(376)_8$ to binary

$(376)_8 = 3 \quad 7 \quad 6$
$011 \quad 111 \quad 110$
$= (011111110)_2$

Binary to Octal Conversion:

→ Convert $(10011010101)_2$ to octal

$(10011010101)_2 = \underbrace{010}_{2}\underbrace{011}_{3}\underbrace{010}_{2}\underbrace{101}_{5} = (2325)_8$

Hexadecimal to Decimal conversion:

→ Convert $A3B_{16}$ to decimal.

$$(A3B)_{16} = A \times 16^2 + 3 \times 16^1 + B \times 16^0$$
$$= 10 \times 16^2 + 3 \times 16^1 + 11 \times 16^0$$
$$= (2619)_{10}$$

Decimal to Hexadecimal conversion:

→ Convert $(235)_{10}$ to hexadecimal

$$(235)_{10} = 16\overline{)235}$$
$$16\overline{)14} \rightarrow 11 \rightarrow B$$
$$0 \rightarrow 14 \rightarrow E$$
$$= (BE)_{16}$$

Hexadecimal to Binary conversion:

→ Convert $(2D5)_{16}$ to binary

$$(2D5)_{16} = \underset{0010}{2} \quad \underset{1101}{D} \quad \underset{0101}{5}$$
$$= (0010\,1101\,0101)_2$$

Binary to Hexadecimal conversion:

→ Convert $(111101101 01)_2$ to hexadecimal

$$(111101101 01)_2 = \underbrace{0111}_{7}\,\underbrace{1011}_{B}\,\underbrace{0101}_{5} = (7B5)_{16}$$

Hexadecimal to Octal Conversion:

→ Convert $(47)_{16}$ to octal

$$(47)_{16} = \underset{0100}{4} \quad \underset{0111}{7}$$
$$= \underbrace{001}_{1}\,\underbrace{000}_{0}\,\underbrace{111}_{7} = (107)_8$$

Octal to Hexadecimal Conversion:

→ Convert $(32)_8$ to hexadecimal

$$(32)_8 = \underset{011}{3} \quad \underset{010}{2} = \underbrace{0001}_{1}\,\underbrace{1010}_{A} = (1A)_{16}$$

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Arithmatic Operation :

Binary Arithmatic :

→

Addition	Substraction	Multiplication	Division
0+0 = 0	0-0 = 0	0×0 = 0	0/1 = 0
0+1 = 1	1-0 = 1	0×1 = 0	1/1 = 1
1+0 = 1	1-1 = 0	1×0 = 0	0/0 = Not allowed
1+1 = 10	10-1 = 1	1×1 = 1	1/0 = Not allowed

Binary Addition :

→ Two binary numbers can be added in the same way as two decimal numbers are added. The addition is carried out from least significant bits & proceeds upto most significant bits.

Decimal	Binary
15	1111
+ 10	+ 1010
25	11001

Binary Substraction :

→ The substraction is carried out from LSB to MSB. When '1' is substracted from '0' a '1' is borrowed from higher significant bit.

Decimal	Binary
9	1001
- 7	- 0111
2	0010

Binary Multiplication :

→ The LSB of the multiplier is taken. If the multiplier bit is '1', the multiplicant is copied as such & if the multiplier bit is '0', the '0' is placed in all bit positions.

→ The next higher significant bit is taken & the product is written with a shift to the left.

→ Step-2 is repeated for all other higher significant bits & each time a left shift is given.

```
  101
x 110
-----
  000
 101
101
-----
11110
```

Binary Division :

→ Division in binary follows the same procedure as division in decimal. Division by 0 is meaningless.

11001 ÷ 101

```
        101
101 ) 11001
      101
      ----
      0101
       101
      ----
      0000
```

1's & 2's Complements :

1's complement :

→ In 1's complement, all 0's are converted to 1's & all 1's are converted to 0's.

11001 —1's→ 00110

2's complement :

→ First determine the 1's complement of given number & then add 1 with LSB.

11001 —1's→ 00110
+ 1
00111 (2's complement)

1's complement substraction :

→ Substraction of binary numbers using 1's complement method allows substraction only by addition. To substract a small number from a larger number,

(i) Determine 1's complement of small no.

(ii) Add this to larger no.

(iii) Remove the carry & add it to the result.

→ Substract $(1010)_2$ from $(1111)_2$ using 1's complement

```
  1111
- 1010
  ----
  0101
```

```
                     1111
1's complement     + 0101
                   ------
       Carry ← (1) 0100
                    └──→ 1
                   +
                   ------
                     0101
```

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→ To subtract a larger number from a smaller number,

(i) Determine 1's complement of larger no.

(ii) Add this to smaller no.

(iii) The answer is the 1's complement of true result & is opposite in sign. There is no carry.

→ Subtract $(1010)_2$ from $(1000)_2$ using 1's complement

$$\begin{array}{r} 1000 \\ -1010 \\ \hline -0010 \end{array}$$

1's complement

$$\begin{array}{r} 1000 \\ +\ 0101 \\ \hline 1101 \end{array} \xrightarrow{1's} 0010$$

2's complement subtraction:

→ To subtract a smaller number from a larger number,

(i) Determine 2's complement of smaller number.

(ii) Add to the larger no.

(iii) Discarded the carry.

→ Subtract $(1010)_2$ from $(1111)_2$ using 2's complement

$$\begin{array}{r} 1111 \\ -1010 \\ \hline 0101 \end{array}$$

2's complement

$$\begin{array}{r} 1111 \\ +\ 0110 \\ \hline \text{Carry} \rightarrow (1)0101 \end{array}$$

$\because 1010 \xrightarrow{1's} 0101$

$$\begin{array}{r} +\ \ 1 \\ \hline 2's \rightarrow 0110 \end{array}$$

→ To subtract a larger number from a smaller number,

(i) Determine 2's complement of larger no.

(ii) Add 2's complement to smaller no.

(iii) There is no carry. The result is in 2's complement form & is negative.

(iv) To get an answer in true form, take the 2's complement & change the sign.

Subtract $(1010)_2$ from $(1000)_2$ using 2's complement

$$\begin{array}{r} 1000 \\ -1010 \\ \hline 0010 \end{array}$$

2's compl.

$$\begin{array}{r} 1000 \\ +\ 0110 \\ \hline 1110 \end{array}$$

$\because 1010 \xrightarrow{1's} 0101$

$$\begin{array}{r} +\ \ 1 \\ \hline 2's \rightarrow 0110 \end{array}$$

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Signed Binary Number Representation:

→ Binary numbers are represented with a separate sign bit along with magnitude.

→ For example, in an 8-bit number, the MSB is the sign bit & remaining 7-bits correspond to magnitude. The magnitude part contains true binary no. for positive no., while 2's complement form of the number for negative no.

$+13 = \underbrace{0}_{\text{sign bit}}\ \underbrace{0001101}_{\text{Magnitude}}$

$-46 = \underbrace{1}_{\text{sign bit}}\ \underbrace{0101110}_{\text{Magnitude}}$

Addition in 2's complement system:

→ When both nos are positive:

$+29$ & $+19$

$+29$: $0\ 0\ 0\ 1\ 1\ 1\ 0\ 1$

$+19$: $+\ 0\ 0\ 0\ 1\ 0\ 0\ 1\ 1$

$+48$: $\therefore\ 0\ 0\ 1\ 1\ 0\ 0\ 0\ 0$

→ Positive addend & Negative addend no.

$+39$ & -22

$+39$: $0\ 0\ 1\ 0\ 0\ 1\ 1\ 1$

-22 : $+\ 1\ 1\ 1\ 0\ 1\ 0\ 1\ 0$

17 : (omit carry) $\rightarrow (1)\ 0\ 0\ 0\ 1\ 0\ 0\ 0\ 1$

First, find $+22$ (00010110) must be converted to 2's complement -22 (11101010)

→ Positive addend & Negative added no.

-47 & $+29$

-47 : $1\ 1\ 0\ 1\ 0\ 0\ 0\ 1$

$+29$: $+\ 0\ 0\ 0\ 1\ 1\ 1\ 0\ 1$

-18 : $1\ 1\ 1\ 0\ 1\ 1\ 1\ 0$ (-18)

First, find $+47$ (00101111) must be converted to 2's complement -47 (11010001). The result is 2's complement of 18.

__/__/____

→ When both no.s are negative.

-32 & -44

```
-32          11100000
-44        + 11010100
-76      (1)10110100   (-76)
```

Omit carry

→ First find +32 (00100000) must be converted to 2's complement -32 (11100000) & +44 (00101100) must be converted to 2's comp. -44 (11010100). The result is 2's complement of 76.

Subtraction in 2's complement system:

→ When both no.s are positive.

+19 is to subtracted from +28.

```
+28  → 00011100
+19  → 00010011
```

First find +19 to a 2's complement, -19 (11101101).

Now add +28 & -19

```
+28          00011100
-19        + 11101101
+09      (1)00001001
```

Omit carry

→ Positive number of minuend & negative no. of subtrahend.

-21 is to subtracted from +39

```
+39 → 00100111
-21 → 11101011
```

First, find -21 to a 2's complement, +21 (00010101).

Now, add +39 & +21

```
+39          00100111
+21        + 00010101
+60          00111100
```

→ Positive number subtrahend & negative no. of minvend.

+19 is to subtracted from -43.

-43 → 1 1 0 1 0 1 0 1

+19 → 0 0 0 1 0 0 1 1

First, find -43 to a 2's complement, +43 (00101011).

Now, add +43 & +19

$$\begin{array}{r} +43 \\ +19 \\ \hline +62 \end{array} \qquad \begin{array}{r} \rightarrow 0\,0\,1\,0\,1\,0\,1\,1 \\ +\;0\,0\,0\,1\,0\,0\,1\,1 \\ \hline 0\,0\,1\,1\,1\,1\,1\,0 \end{array}$$

→ Both the numbers are negative.

-33 is to subtracted from -57.

-57 → 1 1 0 0 0 1 1 1

-33 → 1 1 0 1 1 0 1 1

First, find -33 to a 2's complement, +33 (00100001).

Now, add -57 & +33.

$$\begin{array}{r} -57 \\ +33 \\ \hline -24 \end{array} \qquad \begin{array}{r} \rightarrow 1\,1\,0\,0\,0\,1\,1\,1 \\ +\;0\,0\,1\,0\,0\,0\,0\,1 \\ \hline 1\,1\,1\,0\,1\,0\,0\,0 \end{array}$$

∵ The result is 2's complement of 24.

Comparision between 1's & 2's complements :

→ The 1's complemented can be easily obtained using an inverter. The 2's complement has to be arrived at by first obtaining the 1's complement & then add one (1) to it.

→ The advantages in 2's complement is that only one arithmatic operation is required, the 1's complement requires two operation.

→ While the 1's complement is often used in logical manipulations for inversion operation, the 2's complement is used only for arithmatic applications.

9's & 10's Complement:

9's complement:

→ The 9's complement of a decimal no. can be found by subtracting each digit in the number from 9.

→ Find 9's complement of 469 & 4397.

$$\begin{array}{r} 999 \\ -469 \\ \hline 530 \end{array} \qquad \begin{array}{r} 9999 \\ 4397 \\ \hline 5602 \end{array}$$

9's Complement subtraction:

→ Subtraction of a smaller number from a larger number, the 9's complement system is done by the addition of 9's complement of subtrahend to the minuend & if carry is there then it add with result.

→ Subtraction of a larger number from a smaller number, the 9's complement of subtrahend is add with minuend & as there is no carry so the result is negative in the 9's complement form.

→ Subtraction by using 9's complement;

39-23 & 49-84

$$\begin{array}{r} 39 \\ -23 \\ \hline 16 \end{array}$$

9's complement →

$$\begin{array}{r} 99 \\ 23 \\ \hline 76 \end{array} \qquad \begin{array}{r} 39 \\ +76 \\ \hline 115 \\ \hline 16 \end{array}$$

$$\begin{array}{r} 49 \\ -84 \\ \hline -35 \end{array}$$

9's complement →

$$\begin{array}{r} 99 \\ -84 \\ \hline 15 \end{array} \qquad \begin{array}{r} 49 \\ +15 \\ \hline 64 \end{array}$$

As in result, there is no carry, find 9's complement of 64 & the result is in -ve form.

$$99 - 64 = -35$$

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10's Complement :

→ The 10's complement of a decimal no. is equal to its 9's complement then add 1.

→ Find 10's complement of 46 & 739.

```
  99
- 46
----
  53   → 9's complement of 46
+  1
----
  54   → 10's complement of 46
```

```
  999
- 739
-----
  260   → 9's complement of 739
+   1
-----
  261   → 10's complement of 739
```

10's Complement Subtraction :

→ In the 10's complement subtraction, the minuend is added with 10's complement of subtrahend & carry is dropped.

→ Subtraction by using 10's complement ;

69 - 32 & 347 - 265

```
  69
- 32   → 10's Compl →   99
-----                - 32
  37                 ----
                       67
                     +  1
                     ----
                       68
```

```
  69
+ 68
-----
 137
↑ Omit carry
```

```
  347
- 265   → 10's complement →   999
-----                      - 265
   82                      -----
                             734
                           +   1
                           -----
                             735
```

```
  347
+ 735
-----
 1082
↓ Omit carry.
```

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—: BOOLEAN ALGEBRA :—

→ A collection B containing at least two elements 0 & 1 together with binary operations '+' & '.' & one uniary operation '/' (complement) on the set B & satisfying following four properties for any elements a, b, c of B is called a Boolean Algebra.

(i) $a+b = b+a$ & $a.b = b.a$

(ii) $a+1 = 1$, $a.1 = a$ & $a+0 = a$, $a.0 = 0$

(iii) $a.(b+c) = a.b + a.c$ & $a+(b.c) = (a+b).(a+c)$

(iv) For each a, there exists a' (prime) called complement of a, such that $a+\bar{a} = 1$ & $a.\bar{a} = 0$.

Boolean Logic Operations :

→ A Boolean function is an algebraic expression formed using binary constants, binary variables & basic logical operation symbols. Basic logical operation includes the AND function (logical multiplication), OR function (logical addition) & NOT function (logical complementation).

→ Logical AND Operation :

→ The logical AND operation of two Boolean variables A & B is given by, $Y = A.B$

Inputs		Output
A	B	Y = A.B
0	0	0
0	1	0
1	0	0
1	1	1

→ Logical OR Operation :

→ The logical OR operation of two variables A & B is given by, $Y = A+B$.

Inputs		Output
A	B	Y = A+B
0	0	0
0	1	1
1	0	1
1	1	1

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→ Logical Complementation :

→ The logical inverse operation converts the logical '1' to logical '0' & vice versa. This method is also called NOT operation.

Properties of Boolean Algebra :

→ Commutative Property :

Boolean addition is commutative given by,

$$A+B = B+A$$

Boolean algebra is also commutative over multiplication is given by,

$$A \cdot B = B \cdot A$$

→ Associative Property :

The associative property of addition is given by,

$$A+(B+C) = (A+B)+C$$

The associative law of multiplication is given by

$$A \cdot (B \cdot C) = (A \cdot B) \cdot C$$

→ Distributive Property :

The Boolean addition is distributive over Boolean multiplication is given by

$$A+BC = (A+B)(A+C)$$

Proof, $A+BC = A \cdot 1 + BC$

$= A(1+B) + BC \quad (\because 1+x = 1)$

$= A \cdot 1 + AB + BC$

$= A(1+C) + AB + BC$

$= A \cdot 1 + AC + AB + BC$

$= A \cdot A + AC + AB + BC \quad (\because x \cdot x = x)$

$= A(A+C) + B(A+C)$

$= (A+B)(A+C)$

The Boolean multiplication is also distributive over Boolean addition is given by,

$$A(B+C) = A \cdot B + A \cdot C$$

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→ Absorption Law :

(i) $A + AB = A$

Proof, $A + AB = A \cdot 1 + AB$

$= A(1+B)$ $(\because 1+x = 1)$

$= A \cdot 1 = A$

(ii) $A \cdot (A+B) = A$

Proof, $A \cdot (A+B) = A \cdot A + A \cdot B$

$= A + AB$

$= A(1+B) = A$

(iii) $A + \bar{A}B = A+B$

Proof, $A + \bar{A}B = (A+\bar{A})(A+B)$ $(\because A+BC = (A+B)(A+C))$

$= 1 \cdot (A+B)$

$= A+B$

(iv) $A(\bar{A}+B) = AB$

Proof, $A(\bar{A}+B) = A \cdot \bar{A} + A \cdot B$

$= AB$ $(\because A \cdot \bar{A} = 0)$

→ Consensus Law :

(i) $AB + \bar{A}C + BC = AB + \bar{A}C$

Proof, $AB + \bar{A}C + BC = AB + \bar{A}C + BC \cdot 1$

$= AB + \bar{A}C + BC(A+\bar{A})$

$= AB + \bar{A}C + ABC + \bar{A}BC$

$= AB(1+C) + \bar{A}C(1+B)$

$= AB + \bar{A}C$

(ii) $(A+B)(\bar{A}+C)(B+C) = (A+B)(\bar{A}+C)$

Proof, $(A+B)(\bar{A}+C)(B+C) = (A+B)(\bar{A}+C)(B+C+0)$

$= (A+B)(\bar{A}+C)(B+C+A \cdot \bar{A})$

$= (A+B)(\bar{A}+C)(A+B+C)(\bar{A}+B+C)$

$= (A+B)(A+B+C)(\bar{A}+C)(\bar{A}+C+B)$

$= (A+B)(\bar{A}+C)$ $(\because A(A+B) = A)$

Other laws are,

$\bar{A} = \bar{A}$ & $\bar{\bar{A}} = A$

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DeMorgan's Theorem:

→ The first theorem states that, the complement of a product is equal to the sum of the complements. Then,

$$\overline{A \cdot B} = \bar{A} + \bar{B}$$

→ The second theorem states that, the complement of a sum is equal to the product of the complements. Then,

$$\overline{A + B} = \bar{A} \cdot \bar{B}$$

Simplification of Boolean Expressions Using Algebric Method:

1. Prove, $AB + BC + \bar{B}C = AB + C$

$$\text{L.H.S} = AB + BC + \bar{B}C$$
$$= AB + C(B + \bar{B})$$
$$= AB + C \cdot 1$$
$$= AB + C = \text{R.H.S}$$

2. Simplify, $\bar{A}B + AB + \bar{A} \cdot \bar{B}$

$$\bar{A}B + AB + \bar{A} \cdot \bar{B} = B(A + \bar{A}) + \bar{A}\bar{B}$$
$$= B \cdot 1 + \bar{A}\bar{B}$$
$$= B + \bar{A}\bar{B}$$
$$= \bar{A} + B \qquad (\because A + \bar{A} \cdot B = A + B)$$

3. Simplify, $A + A \cdot \bar{B} + \bar{A} \cdot B$

$$A + A\bar{B} + \bar{A}B = A(1 + \bar{B}) + \bar{A}B$$
$$= A \cdot 1 + \bar{A}B$$
$$= A + B$$

4. Simplify, $AB + \bar{A}\bar{C} + A\bar{B}C(AB + C)$

$$AB + \bar{A}\bar{C} + A\bar{B}C(AB + C) = AB + \bar{A}\bar{C} + A\bar{B}C \cdot AB + A\bar{B}C \cdot C$$
$$= AB + \bar{A}\bar{C} + A\bar{B}C \qquad (\because B \cdot \bar{B} = 0 \ \& \ C \cdot C = C)$$
$$= AB + \bar{A} + \bar{C} + A\bar{B}C$$
$$= A(B + \bar{B}C) + \bar{A} + \bar{C}$$
$$= A(B + C) + \bar{A} + \bar{C}$$
$$= AB + AC + \bar{A} + \bar{C}$$
$$= \bar{A} + AB + \bar{C} + AC$$
$$= \bar{A} + B + \bar{C} + A$$
$$= B + \bar{C} + 1 = 1 \qquad (\because A + \bar{A} = 1)$$

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5. Simplify $Y = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + AB\bar{C}$

$Y = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + AB\bar{C}$

$= \bar{A}\bar{C}(\bar{B}+B) + A\bar{C}(B+\bar{B})$

$= \bar{A}\bar{C} + A\bar{C}$

$= \bar{C}(A+\bar{A})$

$= \bar{C} \cdot 1 = \bar{C}$

6. Simplify $Y = \overline{(AB+\bar{C})(\bar{A}+\bar{B}+C)}$

$Y = \overline{(AB+\bar{C})(\bar{A}+\bar{B}+C)}$

$= \overline{(AB+\bar{C})(\bar{A}\cdot\bar{B}+C)}$

$= \overline{(AB+\bar{A}\bar{B} + ABC + \bar{A}\bar{B}\bar{C} + C\cdot\bar{C}}$

$= \overline{0 + ABC + \bar{A}\bar{B}\bar{C} + 0}$

$= \overline{ABC + \bar{A}\bar{B}\bar{C}}$

$= (\bar{A}+\bar{B}+\bar{C})(\bar{\bar{A}}+\bar{\bar{B}}+\bar{\bar{C}})$

$= (\bar{A}+\bar{B}+\bar{C})(A+B+C)$

7. Simplify $Y = \bar{A}C\overline{(\bar{A}BD)} + \bar{A}B\bar{C}\bar{D} + A\bar{B}C$

$Y = \bar{A}C(\bar{A}BD) + \bar{A}B\bar{C}\bar{D} + A\bar{B}C$

$= \bar{A}C(A+\bar{B}+\bar{D}) + \bar{A}B\bar{C}\bar{D} + A\bar{B}C$

$= A\bar{A}C + \bar{A}\bar{B}C + \bar{A}C\bar{D} + \bar{A}B\bar{C}\bar{D} + A\bar{B}C$

$= \bar{A}\bar{B}C + \bar{A}C\bar{D} + \bar{A}B\bar{C}\bar{D} + A\bar{B}C$ $(\because A\cdot\bar{A} = 0)$

$= \bar{B}C(\bar{A}+A) + \bar{A}\bar{D}(C+B\bar{C})$

$= \bar{B}C + \bar{A}\bar{D}(B+C)$ $(\because A+\bar{A}=1 \;\&\; A+\bar{A}B = A+B)$

8. Simplify $Y = \bar{A}B + ABD + A\bar{B}C\bar{D} + BC$

$Y = \bar{A}B + ABD + A\bar{B}C\bar{D} + BC$

$= B(\bar{A}+AD) + C(B+A\bar{B}\bar{D})$

$= B(\bar{A}+D) + C(B+A\bar{D})$

$= \bar{A}B + BD + BC + AC\bar{D}$

$= \bar{A}B + BD + BC(A+\bar{A}) + AC\bar{D}$ $(\because A+\bar{A}=1)$

$= \bar{A}B + BD + ABC + \bar{A}BC + AC\bar{D}$

$= \bar{A}B(1+C) + BD + ABC + AC\bar{D}$

$= \bar{A}B + BD + ABC + AC\bar{D}$

9. Prove that, $BCD + A\bar{C}\bar{D} + ABD = BCD + A\bar{C}\bar{D} + AB\bar{C}$

L.H.S $= BCD + A\bar{C}\bar{D} + ABD$

$= BCD + A\bar{C}\bar{D} + AB(C+\bar{C})D$

$= BCD + A\bar{C}\bar{D} + ABCD + AB\bar{C}D$

$= BCD(1+A) + A\bar{C}(\bar{D}+DB)$

$= BCD + A\bar{C}(\bar{D}+B)$ $\quad (\because A+\bar{A}B = A+B)$

$= BCD + A\bar{C}\bar{D} + AB\bar{C} = R.H.S.$

10. Prove $(A+B)(\bar{A}\bar{C}+C)(\overline{\bar{B}+AC}) = \bar{A}B$

L.H.S. $= (A+B)(\bar{A}\bar{C}+C)(\overline{\bar{B}+AC})$

$= (A+B)(\bar{A}\bar{C}+C)(\bar{\bar{B}}\cdot\overline{AC})$

$= (A+B)(\bar{A}\bar{C}+C)(B\cdot\overline{AC})$

$= (A\cdot\bar{A}\bar{C} + AC + \bar{A}B\bar{C} + BC)(B(\bar{A}+\bar{C}))$ $\quad [\because \overline{AB} = \bar{A}+\bar{B}]$

$= (AC + \bar{A}B\bar{C} + BC)(\bar{A}B + B\bar{C})$

$= AC\cdot\bar{A}B + AC\cdot B\bar{C} + \bar{A}B\bar{C}\cdot\bar{A}B + \bar{A}B\bar{C}\cdot B\bar{C} + BC\cdot\bar{A}B + BC\cdot B\bar{C}$

$= \bar{A}B\bar{C} + \bar{A}B\bar{C} + \bar{A}BC$ $\quad (\because A\cdot\bar{A}=0,\ B\cdot B = B)$

$= \bar{A}B(\bar{C}+\bar{C}+C)$

$= \bar{A}B(C+\bar{C}) = \bar{A}B = R.H.S$

Logic Gates :

→ A logic gate is an electronic circuit which makes logical decisions. To arrive at these decisions, the most common logic gates used are OR, AND, NOT, NAND and NOR gates. The NAND and NOR gates are called as the Universal gates. The exclusive-OR gate is another logic gate which can be constructed using basic gates such as AND, OR and NOT gates.

→ Logic gates have two or more inputs and only one output except for the NOT gate, which has only one input. The output signal appears only for certain combinations of the input signals.

→ Each gate has a distinct logic symbol and its operation can be described by means of an algebraic function. The relationships between i/p & o/p variable of each gate can be represented in a tabular form called Truth Table.

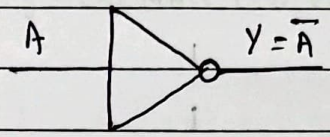
__/__/____

→ NOT Gate :

- It performs a basic logic function called inversion or complementation.
- The purpose of inverter is to change one logic level to opposite level.
- The gate has only one input and one output.

Truth Table

Input	Output
A	$\overline{A}$
0	1
1	0



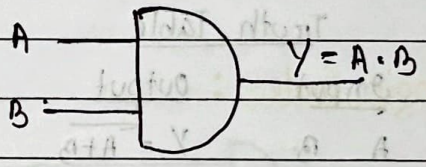
(symbol)

→ AND Gate :

- It performs logic multiplication, know as "AND" function.
- It may have two or more no. of inputs. But one output.

Truth Table

Input		Output
A	B	Y = A.B
0	0	0
0	1	0
1	0	0
1	1	1



(symbol)

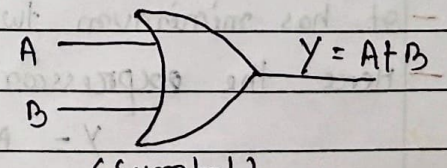
Here output will be "High" if all inputs are "High" otherwise "Low".

→ OR Gate :

- It performs logic addition, know as "OR" function.
- It may have two or more no. of inputs. But one output.

Truth Table

Input		Output
A	B	Y = A+B
0	0	0
0	1	1
1	0	1
1	1	1



(symbol)

- The output is "High" if any of input is "High" otherwise "Low".

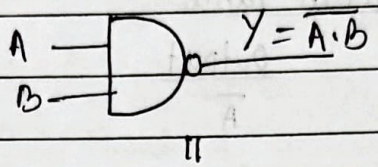
__/__/____

→ NAND Gate:

- The term NAND is a contraction of NOT-AND & implies an AND function with complemented output.
- Here output is "Low" when all inputs are "High" otherwise "High".
- It has minimum two inputs.

Truth Table

Input		Output
A	B	$Y = \overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0



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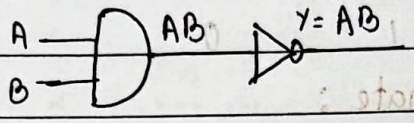
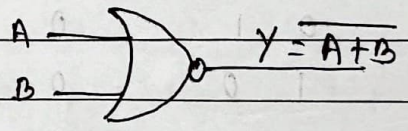


→ NOR Gate:

- The term NOR is a contraction of NOT-OR & implies an OR function with complemented output.
- Here output is "High" when both inputs are "Low" otherwise "Low".
- It has minimum two inputs.

Truth Table

Input		Output
A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0



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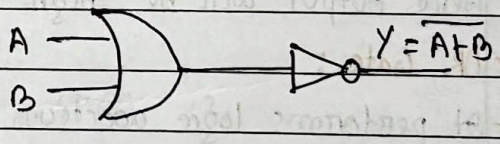
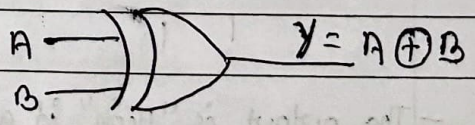


→ Exclusive-OR (X-OR) Gate:

- This gate produce the output, "High" when inputs have odd no. of 1's.
- It has minimum two inputs.
- Here the expression for output is,

$$Y = A \oplus B$$
$$= \bar{A}B + A\bar{B}$$



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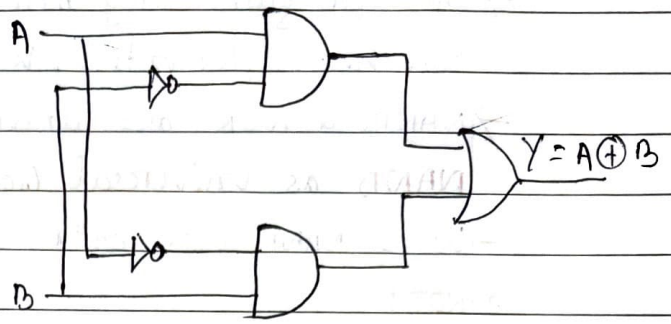
Truth Table

Input		Output
A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

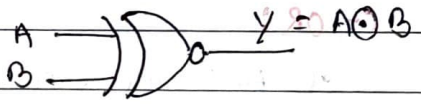


- This is known as even parity-checker in equality comparator or detector.

→ Exclusive-NOR (X-NOR) Gate:

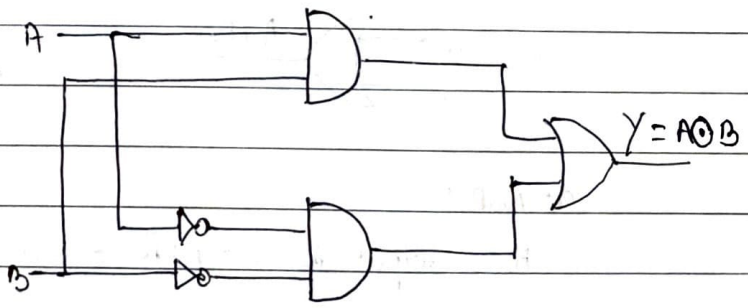
- It is the complement of XOR gate.
- Its output is "High" when number of 1's in the inputs is odd.
- It has minimum two inputs.
- Hence the expression for output is,

$$Y = \overline{A \oplus B}$$
$$= A \odot B$$
$$= AB + \overline{A}\,\overline{B}$$



Truth Table

Input		Output
A	B	$Y = A \odot B$
0	0	1
0	1	0
1	0	0
1	1	1



- It is also known as odd parity checker circuit.

FEEDBACK AMPLIFIER

The process of injecting a fraction of input energy of some vided back to the input is known as feed back

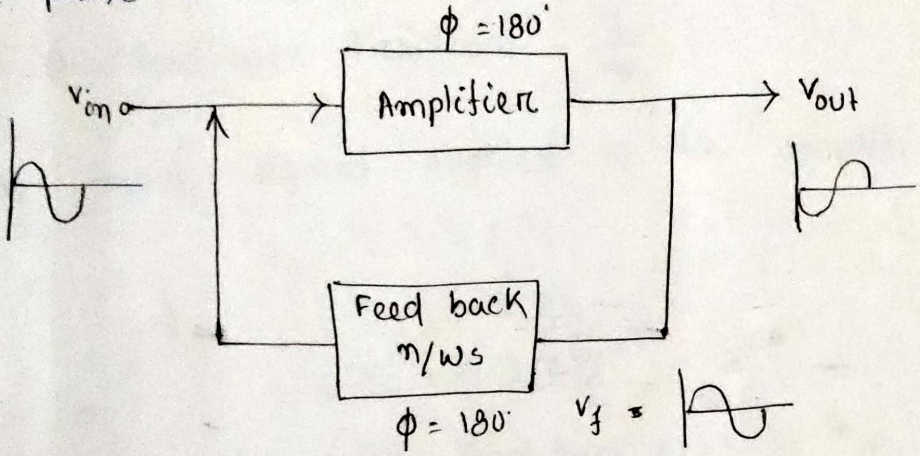
here are two types of feed back ;

(i) +ve feed back (phase shift (ϕ) = 360°)

(ii) -ve feed back (phase shift (ϕ) = 180°)

+ve feed back :—

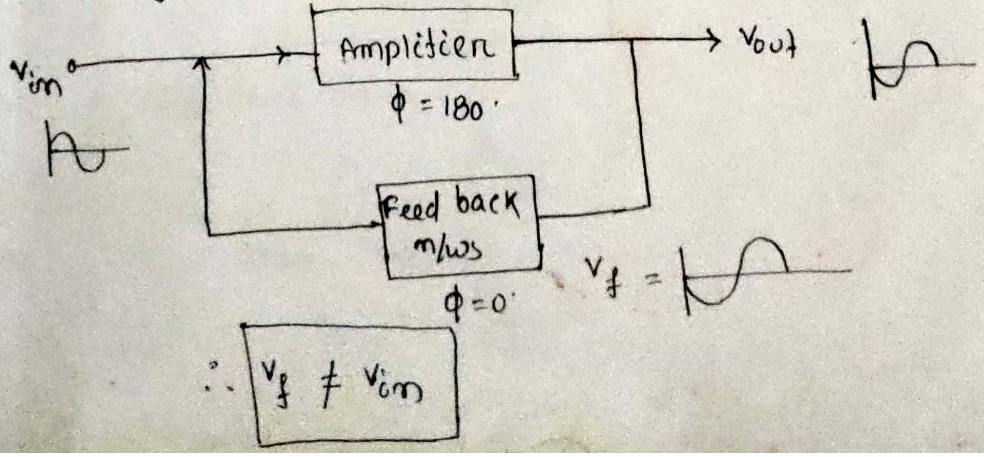
when the feed back energy (voltage & current) is in phase with the input, it is called as +ve feed back. In this case, both amplifier and feed back n/w having phase shift 180°. so that the total phase shift is 360°



$\therefore$ $V_f = V_{in}$

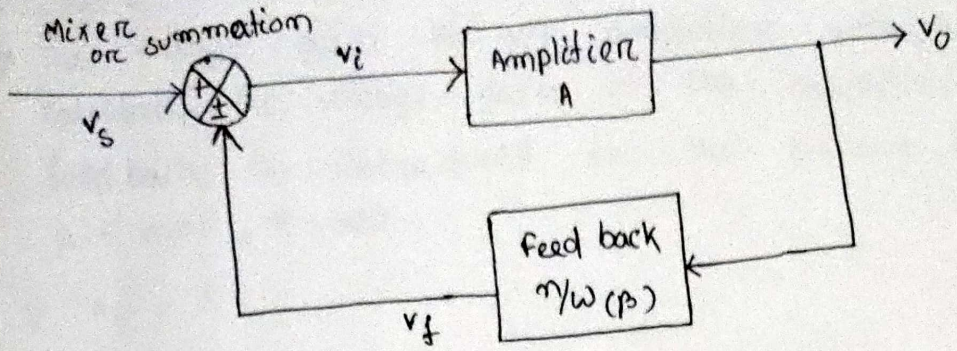
-ve feed back :—

when the feed back energy (voltage & current) is out of phase with the input is called -ve feed back. In this case, the amplifier having the phase shift 180° & the feed back n/w is so design to produce 0° phase shift (ϕ = 0°).



$\therefore$ $V_f \neq V_{in}$

General structure of Feedback Circuit :-



In the figure the amplifier having the gain 'A'.

A = gain without feedback.

$$A = \frac{V_o}{V_i}$$

β = Feed back Fraction $= \frac{V_f}{V_o}$

The input signal applied to the amplifier is

$$V_i = V_s \pm V_f$$

$$\Rightarrow V_i = V_s \pm \beta V_o$$

$$\Rightarrow V_s = V_i \pm \beta V_o$$

Now the gain with feed back (A_f) is given by,

$$A_f = \frac{V_o}{V_s}$$

$$= \frac{V_o}{V_i \mp \beta V_o}$$

$$= \frac{V_o/V_i}{V_i/V_i \mp \beta V_o/V_i}$$

$$\Rightarrow \boxed{A_f = \frac{A}{1 \mp A\beta}}$$

For +ve feed back,

$$A_f = \frac{A}{1 - A\beta}$$

For -ve feed back,

$$A_f = \frac{A}{1 + A\beta}$$

Problem :

1)) The voltage gain of an amplifier without feed back is 300. calculate the voltage gain of the amplifier if -ve voltage feed back is interduced in the circuit. Feed back fraction $\beta = 0.01$, $A = 300$.

⇒ $A_f = ?$

we know -ve feed back ;

$$A_f = \frac{A}{1 + A\beta}$$

given data ,

$A = 300$

$\beta = 0.01$

$$A_f = \frac{300}{1 + 300 \times 0.01}$$

$=$

2)) The overal gain of multistage amplifier is 140 when -ve voltage feed back is applied the gain is reduces to 17.5. Find the fraction of the output .i.e. feed back to the input.

⇒ $\beta = ?$

we know -ve feed back ;

$$A_f = \frac{A}{1 + A\beta}$$

given data ,

$A = 140$

$A_f = 17.5$

$$A_f = \frac{140}{1 + 140 \times \beta}$$

$\Rightarrow 17.5 (1 + 140\beta) = 140$

$\Rightarrow 17.5 + 2450\beta = 140$

$\Rightarrow 2450\beta = 140 - 17.5$

$\Rightarrow \beta = \frac{122.5}{2450} = 0.05$

3) when a -ve feed back voltage is applied to an amplifier of gain 100, the overal gain falls to 50.

(i) calculate the feed back fraction.

(ii) If this fraction is maintain calculate the value of the amplifier gain, if overal gain is to be 75, $\beta = 0.01$.

=> Given data,

$A = 100$

$A_f = 50$

(i) $\beta = ?$

we know -ve feed back,

$$A_f = \frac{A}{1+A\beta}$$

$$\Rightarrow 50 = \frac{100}{1+100\beta}$$

$$\Rightarrow 50(1+100\beta) = 100$$

$$\Rightarrow 50 + 5000\beta = 100$$

$$\Rightarrow 5000\beta = 100 - 50$$

$$\Rightarrow \beta = \frac{50}{5000} = 0.01$$

(ii) $A_f = 75$

$\beta = 0.01$

$A = ?$

$$A_f = \frac{A}{1+A\beta}$$

$$\Rightarrow 75 = \frac{A}{1+A(0.01)}$$

$$\Rightarrow 75(1+0.01A) = A$$

$$\Rightarrow 75 + 0.75A = A$$

$$\Rightarrow 75 = A - 0.75A$$

$$= A(1-0.75)$$

$$= A \times 0.25$$

$$\Rightarrow A = \frac{75}{0.25} = 300$$

4)// with a -ve voltage feedback an amplifier gives an output of 10 volt, with an input of 0.5 volt when feed back is removed it requires to 0.25 V input (i) calculate gain without feedback.
(ii) feed back fraction

⇒ given data

$V_o = 10$ volt

$V_i = 0.25$ volt

$V_s = 0.5$ volt

(i) Gain without feed back

$$A = \frac{V_o}{V_i} = \frac{10}{0.25} = 40$$

(ii) $\beta = ?$

Gain with feed back

$$A_f = \frac{V_o}{V_s} = \frac{10}{0.5} = 20$$

$$\therefore A_f = \frac{A}{1+A\beta}$$

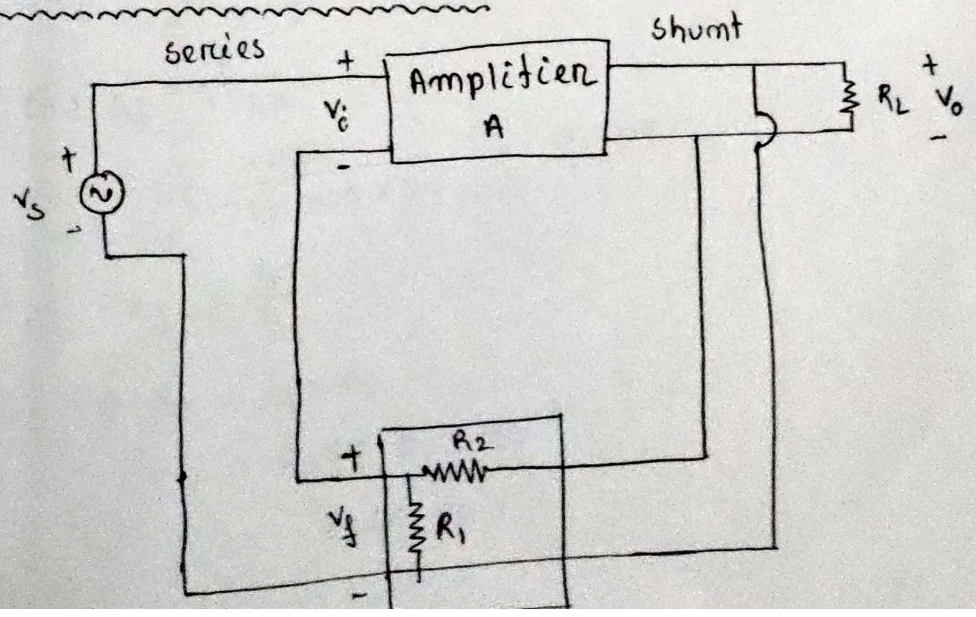
$$\Rightarrow 20 = \frac{40}{1+40\beta}$$

$$\Rightarrow 20 + 800\beta = 40$$

$$\Rightarrow 800\beta = 20$$

$$\Rightarrow \beta = \frac{20}{800} = 0.025 \text{ //}$$

Practical Feedback Circuit :—



$$\beta = \frac{V_f}{V_o}$$

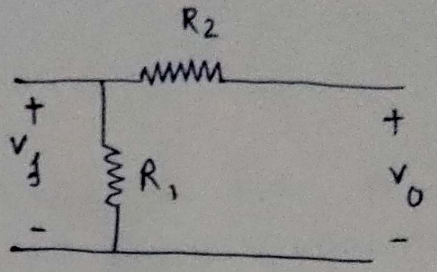
$$\Rightarrow V_f = \beta V_o$$

$\therefore V_f$ = voltage across R_1

$$V_f = \frac{V_o \times R_1}{R_1 + R_2}$$

$$\Rightarrow \frac{V_f}{V_o} = \frac{R_1}{R_1 + R_2}$$

$$\Rightarrow \boxed{\beta = \frac{R_1}{R_1 + R_2}}$$



Problem:

(1) If the gain of the amplifier without feed back is 1000. Find feed back fraction, overal voltage gain & output voltage.

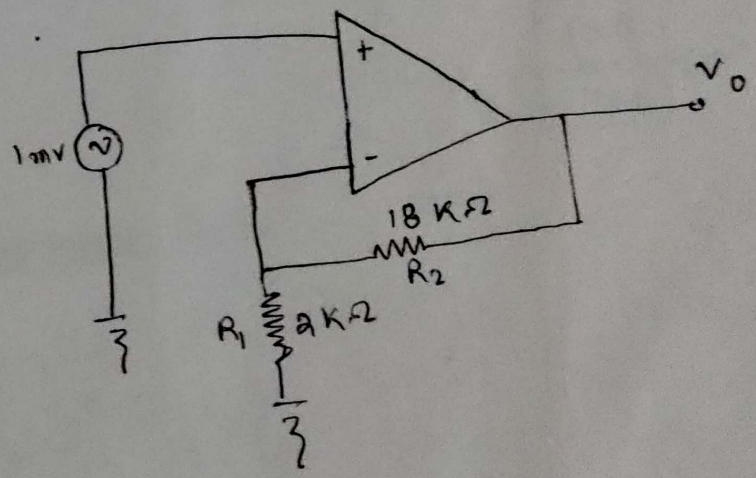
⇒ Given data,

$V_i = 1mV$

$R_1 = 2K\Omega$

$R_2 = 18K\Omega$

$A = 1000$



(i) $\beta = \frac{R_1}{R_1 + R_2}$

$= \frac{2}{2+18} = \frac{2}{20}$

$= 0.1$

(ii) $A_f = \frac{A}{1 + A\beta}$

$= \frac{1000}{1 + 1000 \times 0.1} = 9.99$

(iii) $A_f = \frac{V_o}{V_s}$

$\Rightarrow V_o = A_f \times V_s$

$= 9.99 \times 1 \times 10^{-3}$

$= 9.99\ mV$

Advantages of -ve feed back :—

1- Improve the stability :—

The gain of the -ve feed back, $A_f = \frac{A}{1+A\beta}$.

In this case the feed back factor is $(1+A\beta)$.

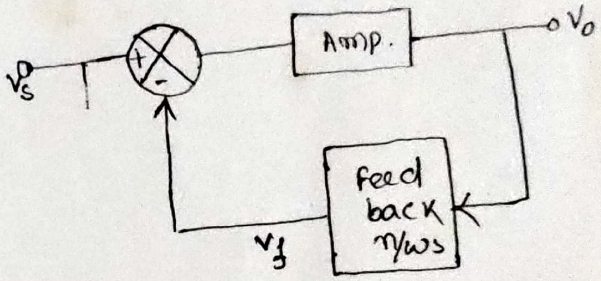
If $A\beta > 1$

$$\therefore A_f = \frac{A}{A\beta} = \frac{1}{\beta}$$

The gain of the feed back depends on β. The gain is unaffected by changes in temp., variation in transistor parameters and frequency. so the gain of the amplifier is stable.

2- Reduction in gain :—

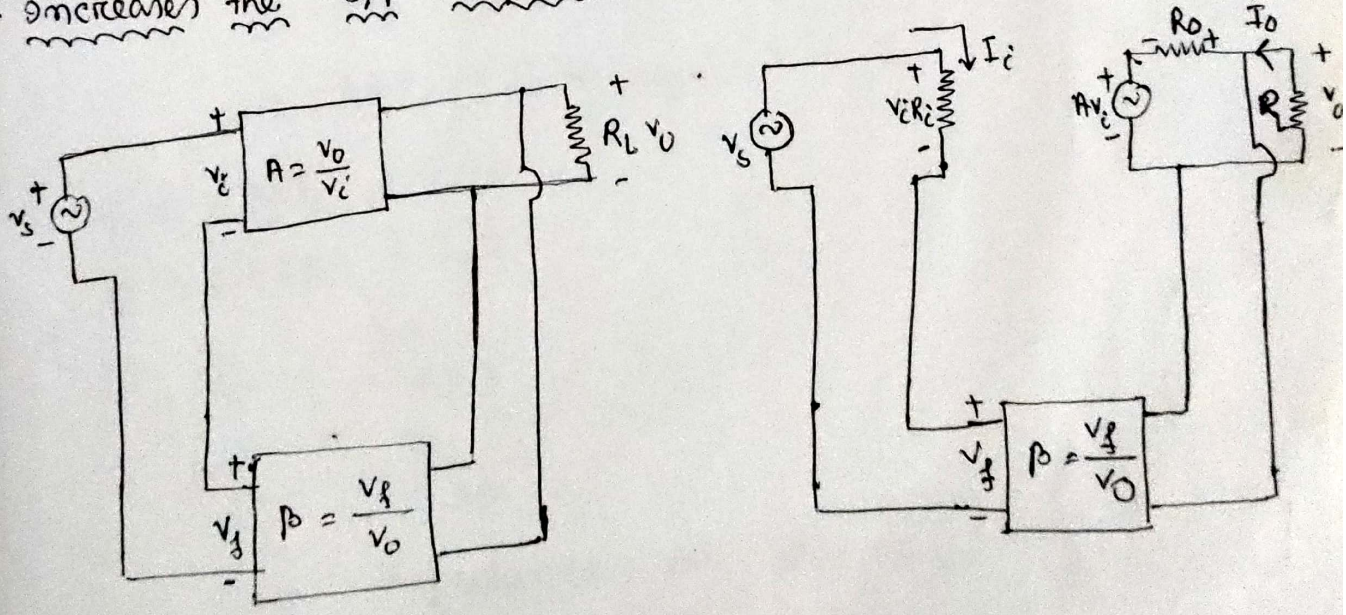
The closed loop gain A_f which is less than that of open loop gain A.



we know;

$$A_f = \frac{A}{1+A\beta}$$

3- Increases the I/P impedance (Z_i) :—



From the O/P side, $V_s = V_i + V_f$

$= V_i + \beta V_o$

$= V_i + \beta A V_i$

$= V_i (1 + A\beta)$

$\Rightarrow V_s = I_i R_i (1+A\beta)$

$\Rightarrow V_s = I_i Z_i (1+A\beta)$

$\Rightarrow \frac{V_s}{I_i} = Z_i$

$= Z_{if}$

As z_i multiplied with the factor $A\beta$. So impedance is increases

4- Decreases of o/p impedance (Z_o) :—

For the o/p analysis take $V_s = 0$

Now $V_s = V_f + V_i$

$\Rightarrow V_i = -V_f$

Applying KVL on o/p side;

$V_o - I_o R_o - AV_i = 0$

$\Rightarrow V_o = AV_i + I_o R_o$

$= -AV_f + I_o Z_o$

$= -A\beta V_o + I_o Z_o$

$\Rightarrow V_o + A\beta V_o = I_o Z_o$

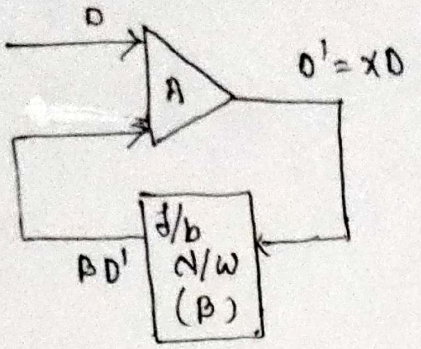
$\Rightarrow V_o (1+A\beta) = I_o Z_o$

$\Rightarrow \frac{V_o}{I_o} = \frac{Z_o}{(1+A\beta)}$

$\Rightarrow Z_{of} = \frac{Z_o}{1+A\beta}$

As o/p impedance is devided with the factor $(1+A\beta)$. So it decreases

Reduction in Distortion :-



Let D = Distortion of the amplifier without feed back

D' : Distortion of the amplifier with feed back.

Assume $D' = xD$ ——— (1)

Fraction of the o/p distontion which is f/b to the input.

$$\beta D' = \beta x D$$

After amplification the distroction becomes $\beta x D A$, it is antiphase with oregional distorcion 'D'.

now $D' = D - \beta x D A$

$$= D(1 - \beta x A) \text{ ——— (2)}$$

compaire eqn (1) & (2) we have

$$xD = D(1 - \beta x A)$$

$$\Rightarrow x = 1 - \beta x A$$

$$\Rightarrow x + \beta x A = 1$$

$$\Rightarrow x(1 + A\beta) = 1$$

$$\Rightarrow \boxed{x = \frac{1}{1 + A\beta}}$$

From eqn (1) $D' = xD$

$$\Rightarrow \boxed{D' = \frac{D}{1 + A\beta}}$$

Problem :-

The gain & distortion of an amplifier 150 & 5%. without feed back. If the stage has 10% of its output voltage applied as -ve feed back. Find the distortion of the amplifier of the feed back.

⇒ Given data,

A = 150

$D = 5\% = 0.05$

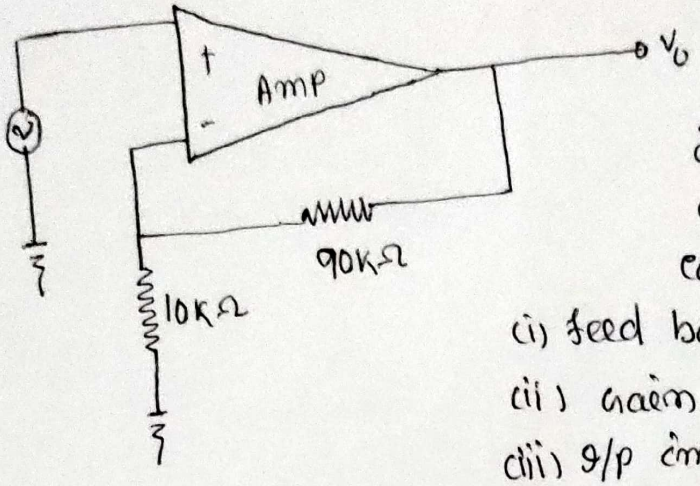
$\beta = 10\% = 0.1$

$$\therefore D' = \frac{D}{1+A\beta} = \frac{0.05}{1+150\times0.1}$$

$$= 3.25 \times 10^{-3}$$

$$= 0.32$$

21)



The gain without f/b is 10000, input impedance is 10KΩ, o/p impedance is 100KΩ. Calculate

(i) feed back fraction

(ii) gain with feed back

(iii) i/p impedance & o/p impedance with feed back.

⇒ Given data,

$A = 10000$ $\quad R_1 = 10K\Omega$

$Z_i = 10K\Omega$ $\quad R_2 = 90K\Omega$

$Z_o = 100K\Omega$

(i) $\beta = \frac{R_1}{R_1+R_2} = \frac{10}{10+90} = 0.1$

(ii) $A_f = \frac{A}{1+A\beta} = \frac{10000}{1+10000\times0.1} = 9.99$

(iii) $Z_{if} = Z_i(1+A\beta)$

$= 10(1+10000\times0.1)$

$= 10010$

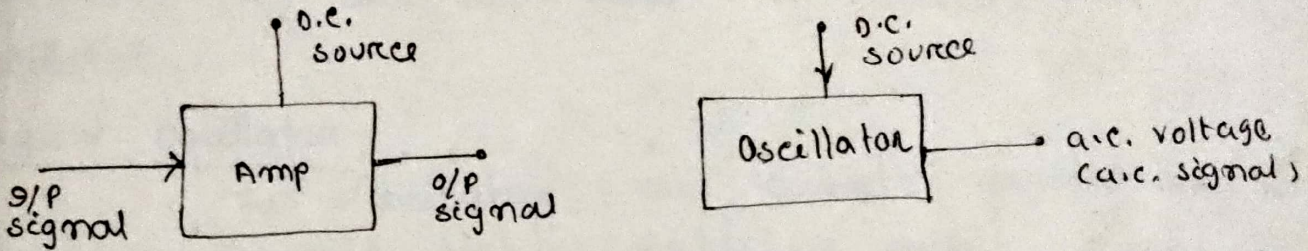
(iv) $Z_{of} = \frac{Z_o}{1+A\beta} = \frac{100}{1+10000\times0.1}$

$= 0.099$

Oscillator

Any circuit which is used to generate an a.c. voltage without ac input signal is called as an oscillator. To generate a.c. voltage, the circuit is supplied energy from a d.c. source. This device gives the frequency ranges from few Hz to several GHz. Generally it is said that oscillator generates a sinusoidal signal.

Comparison between an amplifier and an oscillator :-



An amplifier is an device which produces an output signal with a same wave form as that of input, but its power level is generally high. This additional power is supplied by an external d.c. source. Hence an amplifier is an energy conversion device.

An oscillator is a device which produces an output signal without any input signal. It producing an output signal so long as the d.c. source is applied.

Classification of an Oscillator :-

a) Sinusoidal or Harmonic Oscillator :

The oscillator which provides an output having a sine wave form, is known as sinusoidal oscillator. Its frequency range from 20Hz to 1GHz.

b) Non-sinusoidal / Relaxation Oscillator :

The oscillator which provides an output having square wave, rectangular wave form as known as non-sinusoidal oscillator. Its frequency range from 0Hz to 20MHz.

Types of sinosuidal oscillator :—

a) Tuned circuit Oscillaton :

This oscillatore uses a tuned circuct consist of inductance (L) & capacitance (c) and it is used to generate a high frequency signal. Hence they are also known as radio frequency oscillaton (RF - osc).

b) RC oscillatore :

The oscillaton used resistance (R), capacitor (c) and it is used to generates audio frequency oscillator (AF - osc). They are also known as audio frequency oscillator.

c) Crystal Oscillatore :

This oscillatore uses quartz crystal and it is used to generate highly stablized output signal with frequency upto 10 MHz.

d) -ve Resistance oscillator :

This oscillaton used -ve resistance characteristics of the device such as tunnel diode.

Applicatiom of sinosuidal Oscillator :

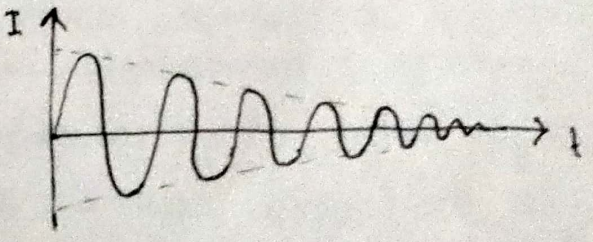
⇒ The most applicatiom in telecommunicatiom is the used of sine wave as a carrien signal.

⇒ The sine wave signal are also used in testing frequency respons of various electronic systems & equipments.

Nature of sinosuidal oscillator :

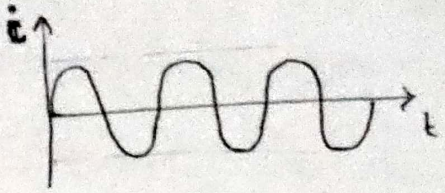
a) Damped Oscillatiom :

The electrical oscillatiom whose amplitude goes on decreasing w.r.t time are known as Damped oscillatiom.



b) Undamped Oscillation :

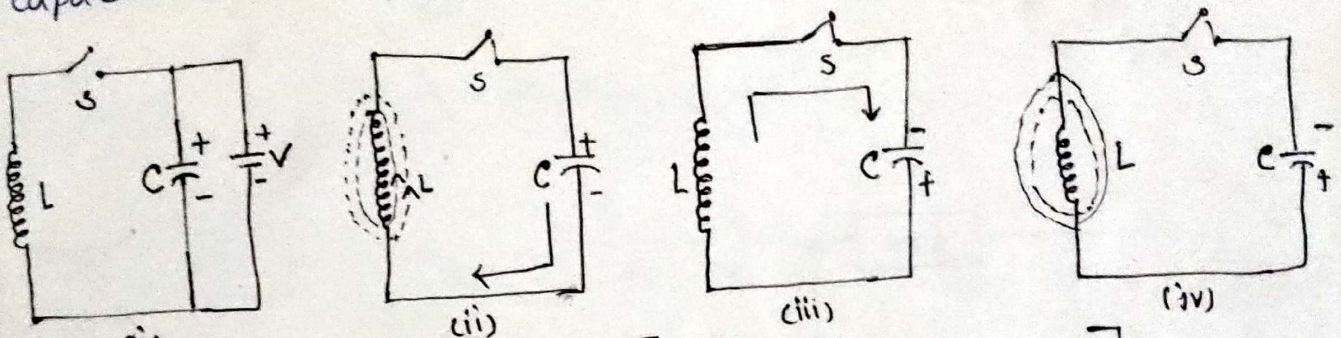
The electrical ascillation whose amplitude remains constant w.r.t time are known as undamped ascillation.



c) Oscillatory circuit (Tank - circuit) :

A circuit which produces electrical oscillation of dry desired frequency is known as Tank circuit.

The tank circuit consists of (L & C) inductance and capacitance which are connected parallely



[In this case electrical energy convert into magnetical energy]

[In this case magnetical energy convert into electrical energy]

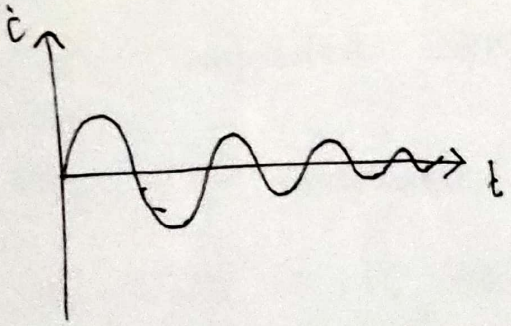


Fig-1 : The upper plate of the capacitor has deflect of electrons and the lower plate has excess of electrons Therefore there is a voltage source connected across a capacitor, it will store the electrostatic energy.

Fig-2 : when switch is closed the capacitor will start to discharge through inductance & the direction of electron as shown in fig. This current will flow in the coil (L) and produces a magnetic field around the coil. so in this fig electrostatic energy is completely converted to magnetic energy.

Circuit Operation :—

When the circuit is switched on, it produces the oscillation of frequency (f). The output of the amplifier which is the feedback to the RC section having the voltage is 'E_0'. This network produces a phase shift of 180 and the voltage is 'E_2' is applied to the amplifier.

The feedback fraction $\beta = \frac{E_2}{E_0}$. A phase shift of 180 which is produce by transistor amplifier. As a result the total phase shift of the circuit is 360.

Advantages :

- It does not required transformer and inductor.
- It can be used to produce very low frequency.
- This circuit provides good frequency stability.

Disadvantages :

- The circuit given very small output

Crystal Oscillator :—

a) Peizo - Electric Crystal :

Crystaline materials like quartz, tourmaline, Rosh salt exhibits the Peizo electric effect (when the voltage applied across them they starts vibrate of the frequency of the applied voltage)

Quartz crystal are generally used in crystal oscillator, because of their greater mechanical strength.

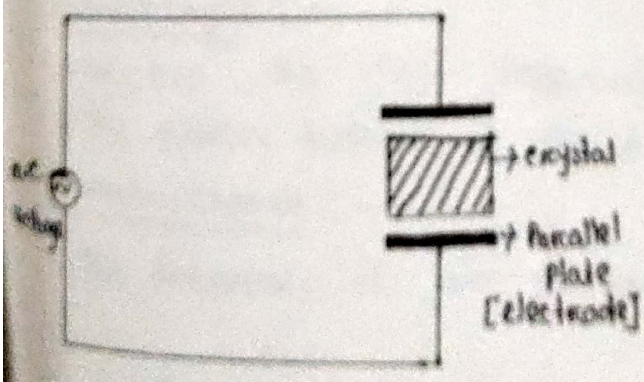
Frequency of the crystal :

The natural frequency of the crystal is given by $F_N = \frac{k}{t}$

where k = constant

t = thickness of the crystal

Working of Quartz Crystal :



The crystal which is placed in between the two parallel plate. The arrangement then forms a capacitor with crystal is the di electric.

If an a.c. voltage is applied across the plate, the crystal will be start vibrating at the frequency of the applied voltage.

Fig-3: once the capacitor is discharge, the magnetic feild will produce an emf. Accordings to the Len's law the emf will keep the current flowing as shown in fig(3).

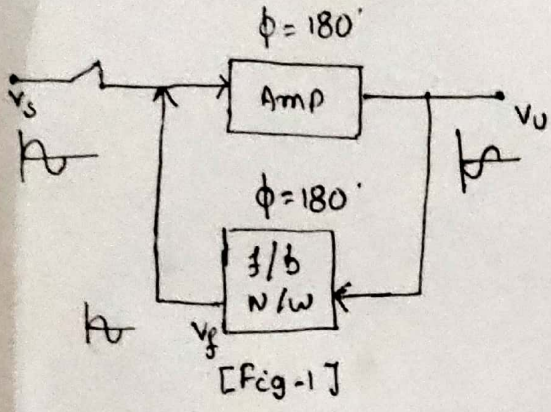
Fig-4: After this the capacitor is again charge. so the magnetic energy is converted into electrostatic energy.

Frequency of Oscillation :

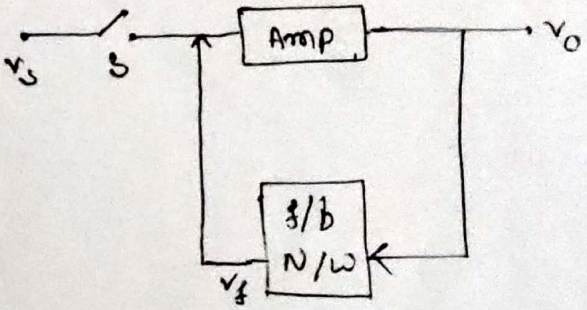
The frequency of oscillation in the tank circuit is determined by the combination of inductance (L) & capacitance (C).

$$\text{Frequency } (f) = \frac{1}{2\pi\sqrt{LC}}$$

+ve Feedback Amplifier - Oscillator :



[Fig-1]



[Fig-2]

A transistor amplifier with the +ve feed back can act an oscillator.

Fig-1: In fig-1, a transistor amplifier with +ve feed back is shown.
when switch is closed V_s is applied to the amplifier and the feedback voltage (V_f) which is equal to the V_s ($V_f = V_0$).
so the total circuit having the phase shift 360° ($\phi = 360°$).

Fig-2: when switch is open that means V_s is removed however V_f which is same phase with V_s is applied to the amplifier. Therefore the amplifier will produce sinusoidal output without external source. Then this +ve feedback amplifier will acts as an oscillator.

In order to get continous undamped output from the circuit, $\boxed{A\beta = 1}$ ——— ①

$\because$ A = Gain without feedback

β = Feedback fraction.

The equation-1 is known as Barkhausen criterion when the oscillator will act as a +ve feedback amplifier. $A_f = \frac{1}{1-A\beta}$

$\therefore A\beta = 1$

$\Rightarrow \boxed{A_f = \infty}$

$\left[\because f = \frac{1}{2\pi RC\sqrt{6}} \right.$
R & C value given $\left. \right]$

RC-phase shift Oscillator :—

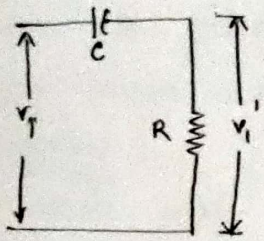


Fig-1

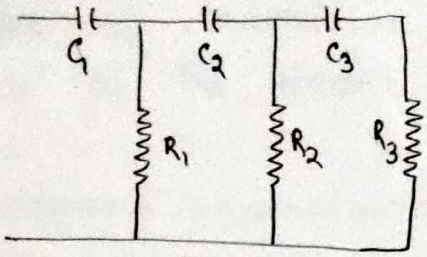


Fig-2

A phase shift circuit consist of a single RC-network which is shown in fig(1). The applied voltage is 'V_i' and the voltage across the resistance ('V_i'') which is load the applied voltage V_i by an phase angle ϕ.

$$\tan\phi = \frac{X_c}{R}$$

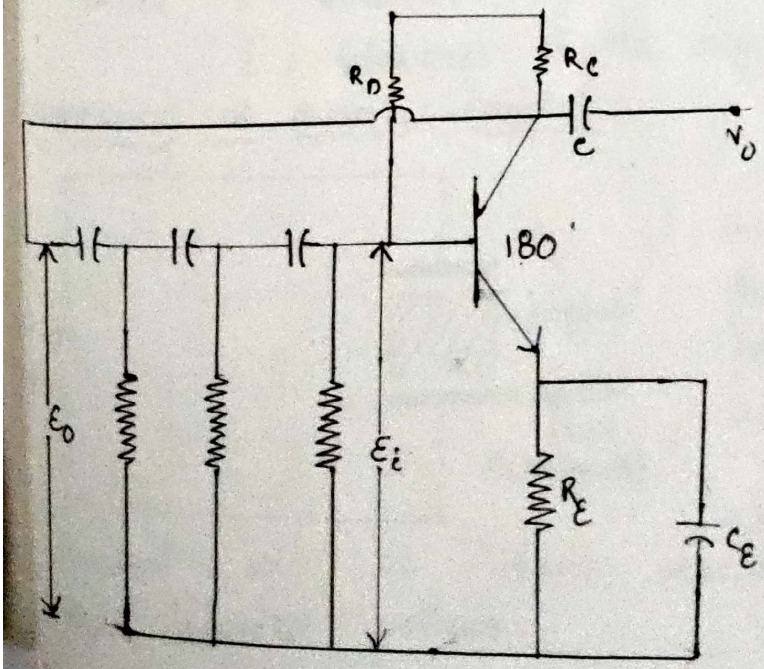
$$\Rightarrow \phi = \tan^{-1}\frac{X_c}{R}$$

$$= \tan^{-1}\frac{1}{\omega CR}$$

If $R = 0$, $\phi = \tan^{-1}\infty = 90^\circ$

But practically $R \neq 0^\circ$. so the value of 'R' will be to get the phase shift, $\phi = 60^\circ$. As a single RC-network will give the phase shift 60°. we have to connect 3 RC-circuit to get a phase shift 180°. ($\phi = 180^\circ$)

Phase-shift Oscillator :—

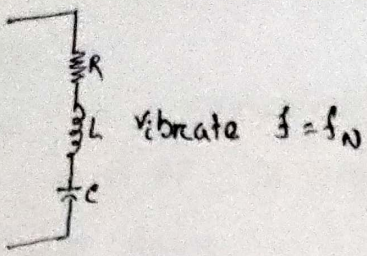


The figure shows the circuit of a RC-phase shift oscillator. The phase shift network consists of R_1C_1, R_2C_2, R_3C_3. At some particular frequency the phase shift in each RC-section is 60°. The frequency of oscillation is given by;

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

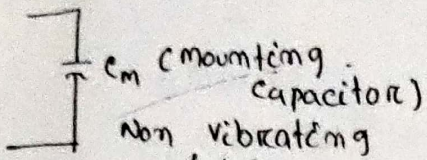
$\therefore R_1 = R_2 = R_3 = R$

$C_1 = C_2 = C_3 = C$

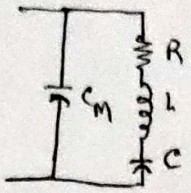


vibrate $f = f_N$

when the crystal is not vibrating, it is equivalent to the capacitance C_M (mountain capacitor) because it has two metal plates separated by the dielectric.



Non vibrating $f \neq f_N$



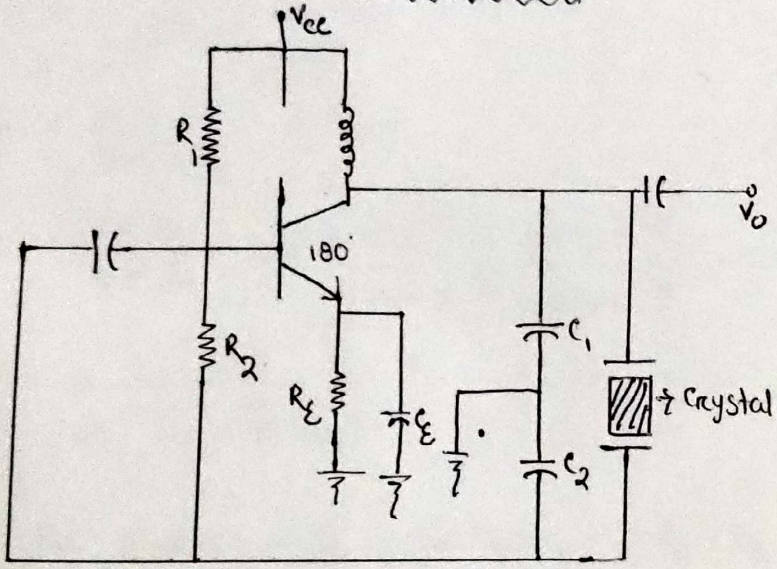
[Equivalent Circuit of Quartz crystal]

f_s (series frequency) $= \frac{1}{2\pi\sqrt{LC}}$

f_p (Parallel frequency) $= \frac{1}{2\pi\sqrt{LC_T}}$

$$\left[\because C_T = \frac{C \times C_M}{C + C_M} \right]$$

TRANSISTOR CRYSTAL OSCILLATOR :—



In this circuit diagram the feed back is the +ve. when the circuit is switched on the transistor will give the phase shift 180° ($\phi = 180°$) and the output of the transistor is again applied to the base of the transistor through the feed back network. As the feed back is +ve, the phase shift of 180° will be produced. Hence the total circuit will produced a phase shift of (ϕ) = 360° and acts as an oscillator.

Advantages :—

→ It has the high frequency stability.

→ The quality factor of the crystal is very high.

Disadvantages :—

→ The frequency of an oscillation can not be change.

Problem :—

1) The a.c. equivalent circuit of a crystal has $L = 1H$, $C = 0.01\ PF$, $R = 1000\ \Omega$, $C_M = 20PF$. Calculate f_s & f_p.

⇒ Given data

$L = 1H$

$C = 0.01\ PF$

$= 0.01 \times 10^{-12}\ F$

$R = 1000\ \Omega$

$C_M = 20\ PF$

$= 20 \times 10^{-12}\ F$

$$f_s = \frac{1}{2\pi\sqrt{LC}}$$

$$= \frac{1}{2\pi\sqrt{1 \times 0.01 \times 10^{-12}}} =$$

$$f_p = \frac{1}{2\pi\sqrt{LC_T}}$$

$$C_T = \frac{C \times C_M}{C + C_M} = \frac{0.01 \times 10^{-12} \times 20 \times 10^{-12}}{0.01 \times 10^{-12} + 20 \times 10^{-12}} = 9.99 \times 10^{-15}\ F$$

$$f_p = \frac{1}{2\pi\sqrt{1 \times 9.99 \times 10^{-15}}} =$$

In the phase shift oscillator $R_1 = R_2 = R_3 = 1M\Omega$, $C_1 = C_2 = C_3 = 68PF$. At what frequency the circuit will oscillate.

⇒ Given data

$R_1 = R_2 = R_3 = R = 1M\Omega = 1 \times 10^6\ \Omega$

$C_1 = C_2 = C_3 = C = 68PF = 68 \times 10^{-12}\ F$

$$f = \frac{1}{2\pi RC\sqrt{6}} = \frac{1}{2\pi \times 1 \times 10^6 \times 68 \times 10^{-12}\sqrt{6}}$$

$=$

SHORT QUESTIONS

BASIC ELECTRONICS.

1. What is the effect of temperature on a semiconductor ?

Sol^{n} :- The effect of temp. on a semiconductor are ;

→ At absolute zero (-273°C) :-

At absolute zero position in a pure semiconductor no free electrons are available as the valence electron are lightly bound in through covelent bonding. So, valence band is full of electrons & covelent band is empty. If in this condition, semiconductor is connected with external battery, no current flows.

→ Above absolute zero :-

If temp. of crystal is raised above absolute zero, few covelent bonds within the crystal are broken due to thermal energy, thus few free electrons are available & they jump from valence band to co-valent band. This empty space is called a hole. If a such crystal is connected with a battery, free electrons will constitute small currents that is called electron current. //

2. What is charge on a semiconductor ?

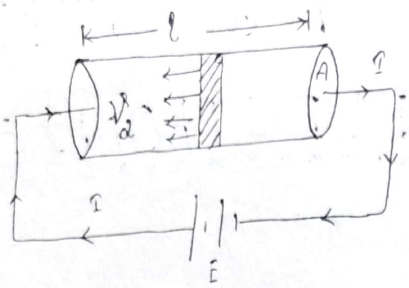
Sol^{n} :- In N-type semiconductor, the number of free electrons is greater than no. of holes. So, this gives us a concept that the N-type semiconductor must be -ve charged. But it is not true because the free electron is provided by Pentavalent atom & atom itself is electrically neutral. Hence, N-type semiconductor is not negative charged but electrically neutral.

Similarly, the P-type semiconductor is also electrically neutral but it carries +ve charged particles called holes. //

3. What is current density in a semiconductor ?

Sol^{n} :- The current flowing per unit area of a conductor is called current density.

$$\Rightarrow J = \frac{dI}{dA}$$



Let, l = length of conductor.

v_d = drift velocity of electron.

n = no. of electrons per unit volume.

No. of electrons = $n \times$ volume

$= n \times A \times l$

Total charge, $q = n \times A \times l \times e$

$= n \times A \times v_d t \times e \quad (\because l = v_d \times t)$

$\Rightarrow \frac{q}{t} = n A v_d e$

$\Rightarrow I = n A v_d e$

$\Rightarrow \frac{I}{A} = n v_d e \quad \Rightarrow J = n v_d e$

$\Rightarrow \boxed{J = n \mu_e e E} \quad (\because v_d = \mu_e E)$ //

4. What is difference between clipper & clamper ?

Sol^n :- clipper :-

A clipper is a circuit with which the waveform is shaped by removing or clipping a portion of applied input signal waveform without distortion the remaining part. clipper can remove signal voltages above or below specified level. It consist of ;

Resistor (R_L), Ideal diode, D.C source.

clamper :-

The circuit that places either positive or negative peak of signal at a desired d.c. level is known as clamping circuit. A clamping circuit should not change peak-to-peak value of the

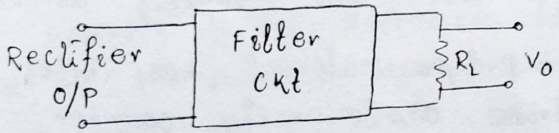
signal, it should only change the d.c level. The operation of clamper is based on the principle that charging time of a capacitor is made very small as compared to its discharging time. It consists of;

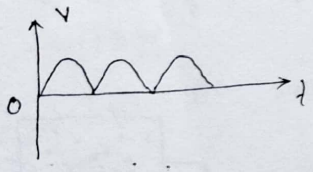
Resistor (R_L), Ideal diode, A capacitor. //

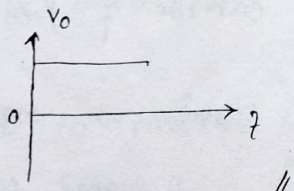
5. What is a filter circuit ?

Sol^n :- The output of rectifier which produces pulsating d.c. (i.e. it contains both a.c. & d.c. components) To get pure d.c., a filter circuit is used which removes the a.c. component & allows the d.c. component to reach the load.

A filter ckt is the combination of inductor & capacitor. A capacitor passes a.c. readily but does not pass d.c at all. An inductor passes d.c. readily but does not pass a.c. at all. Hence, the network L & C can removes a.c. component & allows d.c. component to reach the load.







//

6. What is the conductivity of N-type & P-type semiconductor ?

Sol^n :- From current density of semiconductor;

$$\Rightarrow J = n\mu_e e E$$

$$\Rightarrow J = \sigma E$$

where,

$\sigma = n\mu_e e$ = conductivity.

In pure S.C., even at room temp covelent bond breaks release electron-hole pair. Hence, total current,

$$\Rightarrow I = I_e + I_h$$

Divide A on both sides,

$$\Rightarrow \frac{I}{A} = \frac{I_e}{A} + \frac{I_h}{A}$$

$$\Rightarrow J = J_e + J_h$$

$= n e \mu_e E + n h \mu_h E$

$\Rightarrow \delta \cancel{\ell} = n \cancel{\ell} (\mu_e e + \mu_h h)$

$\Rightarrow \delta = n \mu_e e + n h \mu_h$

where, μ_e = conductivity of electrons.

μ_h = conductivity of holes. //

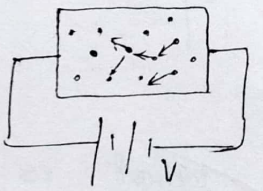
7. What is the majority & minority carrier of a semiconductor ?

Sol^n :- The N-type material has large no. of free electrons where as P-type material has large no. of holes. At room temp., some of covelent bond breaks & thus gives equal no. of free electrons & holes. As N-type material has its share of electron-hole pairs but more no. of electrons present due to effect of impurity. So, N-type material has electrons are majority carrier & holes are minority carrier.

Similarly, P-type material has holes are majority carrier & free electrons are minority carrier. //

8. What is mobility of an electron ?

Sol^n :- A good conductors have plenty of free electrons moving randomly in between the fixed positive ion cores.



When an electric field is applied to a conductor at room temp. electron moves towards the positive terminal of the applied voltage & then continously collide with each other atoms along the way. At each collide, the electron losses some kinetic energy, then accelarates again, gains some velocity in the direction 'E' & loss the energy in next collision. consequently, the electrons gains an average directed drift velocity 'v' which is directly proportional to 'E'.

$\Rightarrow \boxed{v = \mu_e E}$

$\because \mu_e$ = mobility of electrons. //

9. What is zener diode ?

Sol^{n} :- When the reverse bias on a crystal diode increases a critical voltage called breakdown voltage is reached where the reverse current increases sharply to a high value. Therefore, breakdown voltage sometimes called zener voltage & suddenly increases in current is known as zener current.

The zener voltage depends upon amount of doping. If diode is heavily doped, depletion layer will be thin & the breakdown of the junction will occur at lower reverse voltage. If diode is lightly doped, diode has a higher breakdown voltage.

A properly doped crystal doped which has a sharp breakdown voltage is known as zener diode. //

10. Zener diode is always operated in reverse biasing. why ?

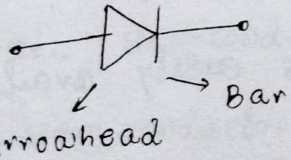
Sol^{n} :- The zener voltage depends upon amount of doping. If diode is heavily doped, depletion layer will be thin & the breakdown of the junction will occur at lower reverse voltage. If diode is lightly doped, diode has higher breakdown voltage.

So, zener diode is always operated in reverse bias. //

11. What is a crystal diode ?

Sol^{n} :- A pn-junction is known as semiconductor or crystal diode.

The main property of crystal diode to conduct current in one direction only permits it to be used as a rectifier.

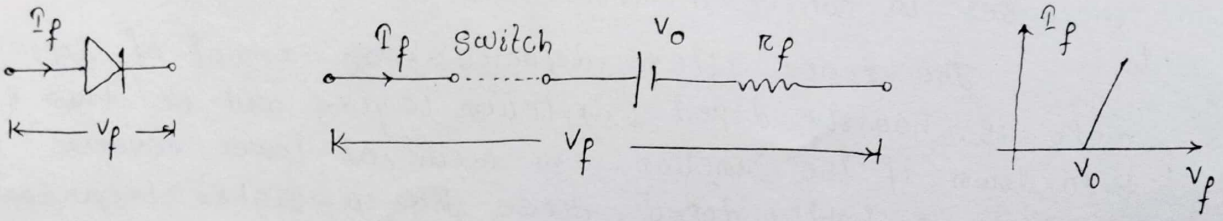


If arrowhead of diode is +ve w.r.t bar, the diode is forward biased.

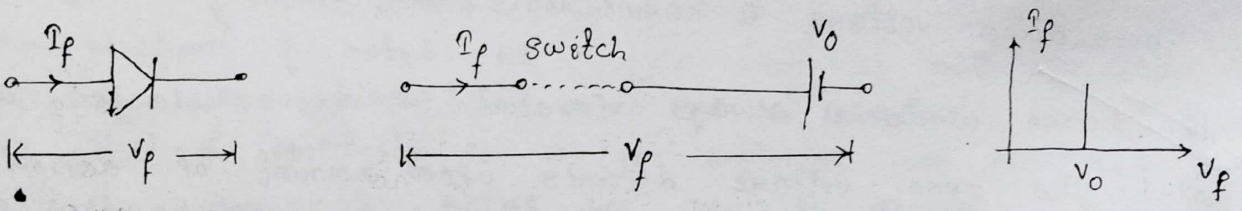
If arrowhead of diode is -ve w.r.t bar, the diode is reverse biased. //

12. Explain equivalent circuit of diode ?

Sol^{n} :- ⇒ Approximate eq. ckt :- when forward voltage V_f is applied across a diode, it will not conduct till the potential barrier V_0 at junction overcome. when V_f exceeds the V_0, diode starts conducting & current I_f is flowing through the diode cause voltage drop internal resistance R_f.



⇒ Simplified eq. ckt :- The internal resistance R_f can be ignored as compared to other elements.



⇒ Ideal diode :-

An ideal diode is one which behaves as a perfect conductor when forward bias & as a perfect insulator when reverse bias. So, $R_f = 0$ & V_0 is negligible.

13. Which are most commonly used semiconductor & why ?

Sol^{n} :- Silicon is commonly used most of the time as compared to Germanium because ;

⇒ Being an ore of silicon is easily available on earth.

⇒ It has low cost.

⇒ This power dissipated by silicon is very-very less.

⇒ It can be operated by high temp. i.e. 150°C but germanium is operated by 70°C.

14. Distinguish between avalanche & zener breakdown ?

Sol^{n} :-

⇒ Avalanche breakdown :-

This type of breakdown takes place in devices with thicker junction like ordinary semiconductor diodes. In this breakdown voltage, electric field of the depletion layer becomes very high such that at high reverse voltage, electrons acquire very high velocity that they dislodge valence electron from semiconductor atom. The field at the depletion layer attains such a high value that an infinite large current flows which breaks down the junction permanently.

⇒ Zener breakdown :-

This type of breakdown takes place in devices with thin depletion layer like zener diode. In this breakdown the electric field at the depletion layer becomes very large with a very small reverse bias. A small number of electrons jump across the barrier & zener breakdown occurs. In this breakdown the junction is not damaged permanently. If the reverse bias is removed, the device can its original position. //

15. What is intrinsic semiconductor ?

Sol^{n} :- A pure semiconductor is called intrinsic semiconductor. At absolute zero temp., a pure semiconductor behaves as an insulator. If its temp. is raised, the covelent bonds are broken. So, it produces electrons & holes. Therefore, concentration of electrons & holes in an intrinsic semiconductor will always be equal. The total current in the semiconductor is equal to current due to electrons & holes. //

16. What is extrinsic semiconductor ?

Sol^{n} :- The intrinsic semiconductor has very less conduction capacity. But in electronic devices we require the conduction capacity should be increased a little beat. This can be obtained by addition of metallic impurity to the semiconductor According to this, we have to select a suitable impurity & add. It is 2 types :

✓N - type & P - type semiconductor. //

17. What is doping ?

Soln :- Intrinsic semiconductor by itself is of little significance as it has little current conduction capacity at ordinary room temp. but if very small amount of impurity is added to it in the process of crystallisation, the electrical conductivity increased many times & addition process is known as doping. //

18. Define diffusion of current in a semiconductor ?

Soln :- The diffusion of charge carriers is as a result of a gradient of carrier concentration. In this case, concentration of charge carrier (either electron or hole) tend to distribute themselves uniformly throughout the semiconductor crystal. This movement continues until all the carriers are evenly distributed throughout the material. This type of movement of charge carriers is called diffusion current. //

19. What is energy gap ?

Soln :- The energy gap between the valence band & conduction band is known as forbidden energy gap. Forbidden energy gap is a region in which no electron can stay as there is no allowed energy state. The greater the energy gap more tightly the valence electrons are bound to the nucleus. //

20. What is meant by fermi-level in a semiconductor ?

Soln :- Fermi-level in a semiconductor can be defined as the maximum energy that an electron in a semiconductor have a zero degree absolute. //

21. What is the effect of temp. on extrinsic semiconductor ?

Soln :- With the increase in temp. of extrinsic semiconductor, the number of thermally generated carriers is increased resulting in increase of concentration of minority carriers. At temp. exceeding critical temp. the extrinsic semiconductor behaves like an extrinsic semiconductor but with higher conductivity. //

22. What do you understand by reverse saturation current of a diode ?

Sol^{n} :- Reverse saturation current of a diode is due to minority carriers & is caused when the diode is reverse biased. only a very small voltage required to direct all minority carriers along the junction & when all minority carriers are flowing across further increase in bias voltage will not cause increase in current. This current is referred to as a reverse current. //

23. Define α & β for a transistor ?

Sol^{n} :-

$\Rightarrow \alpha$:- It is the d.c. current gain & is equal to the ratio of collector current to emitter current.

$\Rightarrow \beta$:- It is the current gain factor of a common-emitter circuit & is defined as the ratio of collector current to base current. //

24. Which of the following can be used as impurity of n-type semiconductors ?

gallium, arsenide, phosphorous, germination, antimony ?

Sol^{n} :- Phosphorous & antimony can be used as impurity of n-type semiconductors. //

25. Why Silicon diodes are used as rectifiers ?

Sol^{n} :- Rectifiers are the circuit which converts alternating current to unidirectional current or d.c. current i.e. the direction to flow of current through load resistance is always in one direction. As diodes are unidirectional current device i.e. current is always flow from P to N during forward biased condition, diodes are used as a rectifiers. Again Si has various advantages over Ge due to its high temp. with standing capabilities & high peak inverse voltage. Hence, silicon diodes are used as rectifiers. //

26. Explain why capacitors help in filtering ?

Sol^{n} :- When ever capacitors are used in a circuit it offers reactance given by, $X_C = \frac{1}{2\pi f_C}$. Again for DC, $f = 0$ HZ & $X_C = \infty \Omega$ & for AC, f = finite value & X_C = some finite value $< \infty \Omega$ thus capacitor provide a high resistance for DC & path will be open circuited. similarly, for ac the resistance is very less & the path will be short circuited. Therefore when ever capacitor is used all the d.c. component will be blocked & the a.c. component will pass, thus help in filtering. //

27. How current flow in a semiconductor is different from that in a metal ? Explain.

Sol^{n} :- In case of semiconductor, the current flow due to flow of both electrons & holes, but for metals current flows due to flow of electrons only. Semiconductors have negative temp. coefficient of resistance but metals have positive temp. coefficient of resistance. //

28. Define the volt equivalent of temperature ?

Sol^{n} :- volt equivalent of temp. is defined by,

$$V_T = \frac{KT}{q} = \frac{T}{11,600}$$

Where, K = Boltzman's constant.

T = Temp. in ^{0}K.

q = charge of an electron = 1.602×10^{-19} C.

29. Is the temperature coefficient of resistance of a metal positive or negative, explain ?

Sol^{n} :- A metal has positive temp. coefficient of resistance because at room temp. a conductor has all possible free electrons. So, additional thermal energy due to temperature doesn't produce any more electrons start moving faster & the atom starts vibrating. As a result the electrons experience more collisions. Because of more ~~in~~hinderance in the motion of free electrons at higher temp., the resistance of metal increases. //

30. What is an integrated circuit ? write the advantages & disadvantages of ICs ?

Sol^{n} :- An IC is a complete electronic circuit in which both active & passive components are fabricated on a single chip of silicon.

Advantages :-

→ Extremely small physical size.
→ Extremely high reliability.
→ very small weight.
→ Reduced cost.
→ Easy replacement & low power consumption.

Disadvantages :-

→ coils or transformer can't be fabricated.
→ They handle only limited amount of power.
→ IC function at fairly low voltages. //

31. What are the different classifications of ICs ?

Sol^{n} :- ⇒ Depending scale of integration :-

(a) SSI < 10 component
(b) MSI < 100 (c) LSI < 10,000
(d) VLSI 10,000 - 99,999.

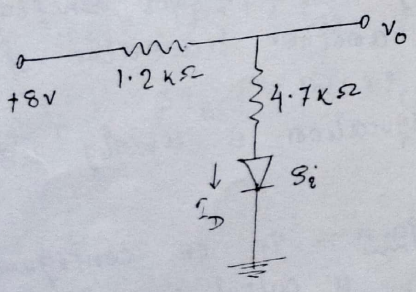
⇒ classification as per structure :-

(a) monolithic IC
(b) Hybrid ICs.

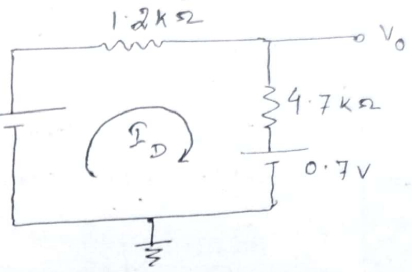
⇒ classification as per application :-

(a) liner IC (b) Digital. //

32. Determine V_o & I_D for the given network ;



Sol^n :-

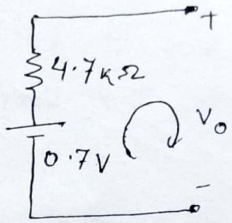


Apply KVL,

$8V - 1.2 \times I_D - 4.7 \times I_D - 0.7 = 0$

$\Rightarrow I_D = 1.24\ mA$

Again Apply KVL,



$0.7V - 4.7\ K\Omega \times I_D - V_o = 0$

$\Rightarrow V_o = 0.7 - 4.7\ K\Omega \times 1.24\ mA$

$= 6.51\ V.$ //

33. what is meant by operating point ?

Sol^n :- The zero signal values (no a.c. signal is applied) of collector current I_C & collector-to-emitter voltage V_{CE} are called as the operating point.

This point is also called quiescent (stable) point or Q-point since it is a point on output characteristics curve when the transistor is in a silent condition (i.e. the absence of a.c. input signal). //

34. What is need of transistor biasing ?

Sol^n :- A. A biasing must set the operating point in the middle of active region of the transistor characteristic

B. A biasing circuit must stabilize the collector current against temp. variations.

C. A biasing circuit must ensure that the operating poi is independent of transistor parameters such as β so that operating point is not shifted if the transisto is replaced by another transistor of same type. //

35. Why is CE configuration is widely used in transistor application ?

Sol^n :- A. High current gain :- In CE configuration, I_B is input current & I_C is output current. So,

$\Rightarrow I_C = \beta I_B + I_{CEO}$

As β is very large. So, I_C is more than I_B. So, current gain is high.

B. High voltage & Power gain :-

Due to high current gain, voltage & Power gain is also high.

C. Ratio of o/p & i/p impedances :- In CE configuration, the ratio of output & input impedance is very small. In other configuration, this ratio is very large. //

36. Derive an expression for current amplification & collector current for CE configuration with special reference I_{CEO} ?

Sol^n :- In CE configuration,

current amplification factor, $\beta = \frac{\Delta I_C}{\Delta I_B}$

The collector current (I_C) for CB,

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO} \longrightarrow (1)$$

$$= \beta I_B + I_{leakage} \qquad \left(\because \beta = \frac{\alpha}{1-\alpha}\right)$$

In the above expression, $I_B = 0$, the whole base current does not reach the collector side. There is some leakage current I_{CEO} due to movement of charge carriers across from collector to emitter.

$$\Rightarrow I_C = \beta I_B + I_{CEO}$$

$$\therefore I_{CEO} = \frac{1}{1-\alpha} I_{CBO}$$

we know, $\beta = \frac{\alpha}{1-\alpha} \Rightarrow \beta + 1 = \frac{\alpha}{1-\alpha} + 1$

$$\Rightarrow \beta + 1 = \frac{1}{1-\alpha}$$

So, $I_{CEO} = (\beta + 1) I_{CBO}$

Now, $I_C = \beta I_B + (\beta + 1) I_{CBO}$ //

37. Derive an expression for current amplification & collector current for CC configuration ?

Soln :- In cc configuration,

current amplification factor, $r = \frac{\Delta I_E}{\Delta I_B}$

we know,

$$I_C = \alpha I_E + I_{CBO}$$

& $I_E = I_B + I_C$

$$= I_B + \alpha I_E + I_{CBO}$$

$$\Rightarrow I_E - \alpha I_E = I_B + I_{CBO}$$

$$\Rightarrow I_E (1 - \alpha) = I_B + I_{CBO}$$

$$\Rightarrow I_E = \frac{1}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$$

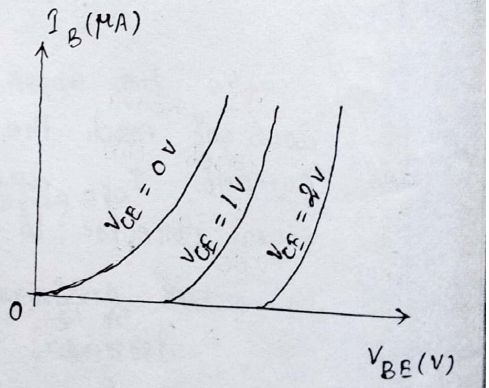
$$\Rightarrow I_E = (\beta + 1) I_B + (\beta + 1) I_{CBO} \quad //$$

38. Draw the input & output characteristic of CE configuration?

Soln :-

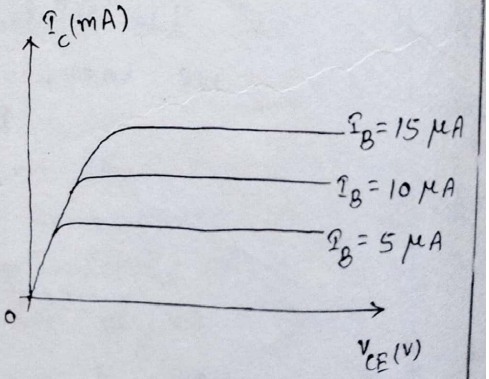
A. Input char. :-

This is the characteristic for the input side & is the curve between base current (I_B) & base emitter voltage (V_{BE}) at const. V_{CE}.



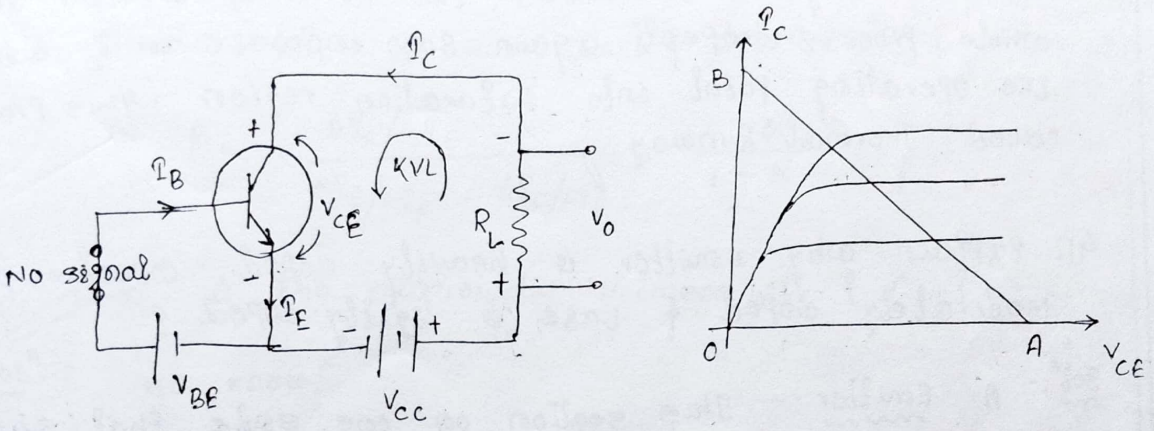
B. output char. :-

This is the characteristic for the output side & is the curve between collector-emitter voltage (V_{CE}) & collector current (I_C) at const. I_B. //



39. What do you mean by load line ? How a D.C. load line draw a output characteristic of a transistor in CE configuration ?

Sol^{n}:- The concept of load line is very important in understanding the working of transistor. It is defined as the locus of operating point on the output characteristic of transistor. It is the line on which the operating point moves when an ac signal is applied to the transistor.



The above ckt shows the CE N-P-N transistor in which no signal is applied between base & emitter & supply voltage V_{cc} is applied at o/p.

Apply KVL at o/p we get.

$$\Rightarrow V_{cc} - I_C R_C - V_{CE} = 0$$

$$\Rightarrow V_{CE} = V_{cc} - I_C R_C \longrightarrow (1)$$

(i) when $I_C = 0$, V_{CE} is max^{m}

$$\Rightarrow V_{CE} = V_{cc}$$

This gives the point A on x-axis.

(ii) when $V_{CE} = 0$, I_C is max^{m}

$$\Rightarrow V_{cc} = I_C R_C$$

$$\Rightarrow I_C = V_{cc}/R_C$$

This gives the point B on y-axis. //

40. What do you mean by Thermal [illegible] transistor ?

Soln:- we know,

$$I_C = \beta I_B + (\beta + 1) I_{CBO}$$

If temp. changes then I_{CBO} changes which in turn chang I_C & operating point. Flow of collector current in the collector circuit produces heat at collector junction. This raises the temp. Hence, I_{CBO} increases which in turn increa I_C. This again increases the temp. of collector junction & whole process repeats again. So, increase in I_C will drive the operating point into saturation region. This process is called Thermal Runway. //

41. Explain why emitter is heavily doped, collector is moderately doped & base is lightly doped ?

Soln:- A. Emitter :- This section on one side that supplies charge carriers (electrons or holes) is called the emitter. The emitter is always forward biased w.r.t base. As it can inject large number of charge carriers. so, emitter is heavily doped.

B. Base :- The middle section of emitter & collector is known as base. The emitter - base junction is forward biased, allowin low resistance for emitter circuit. The base - collector jun^n is reverse biased & provides high resistance in collector circuit. Base is lightly doped & very thin.

C. Collector :- The section on the other other sides collects charge is called collector. The collector is always reverse biased. As collector collect the charge carriers from base so, it is moderately doped. //

42. What is relationship between α & β ?

Soln:- we know,

From CB, $\alpha = \frac{\Delta I_C}{\Delta I_E}$

From CE, $\beta = \frac{\Delta I_C}{\Delta I_B}$

$I_E = I_B + I_C$

$\Rightarrow \Delta I_E = \Delta I_B + \Delta I_C$

$\Rightarrow \Delta I_B = \Delta I_E - \Delta I_C$

$\Rightarrow \frac{\Delta I_C}{\beta} = \Delta I_E - \Delta I_C \quad \left(\because \beta = \frac{\Delta I_C}{\Delta I_B} \Rightarrow \Delta I_B = \frac{\Delta I_C}{\beta}\right)$

$\Rightarrow \beta = \frac{\Delta I_C}{\Delta I_E - \Delta I_C}$

Divide ΔI_E on numerator & denominator:

$\Rightarrow \beta = \frac{\Delta I_C / \Delta I_E}{\Delta I_E/\Delta I_E - \Delta I_C/\Delta I_E} = \frac{\alpha}{1-\alpha}$ //

43. ~~what~~ is the relationship between α & r ?

Sol^n :- we know,

From CB, $\alpha = \frac{\Delta I_C}{\Delta I_E}$

From CC, $r = \frac{\Delta I_E}{\Delta I_B}$

$I_E = I_B + I_C$

$\Rightarrow \Delta I_E = \Delta I_B + \Delta I_C$

$\Rightarrow \Delta I_B = \Delta I_E - \Delta I_C$

$\Rightarrow \frac{\Delta I_E}{r} = \Delta I_E - \Delta I_C \quad \left(\because r = \frac{\Delta I_E}{\Delta I_B} \Rightarrow \Delta I_B = \frac{\Delta I_E}{r}\right)$

$\Rightarrow r = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$

Divide ΔI_E on numerator & denominator;

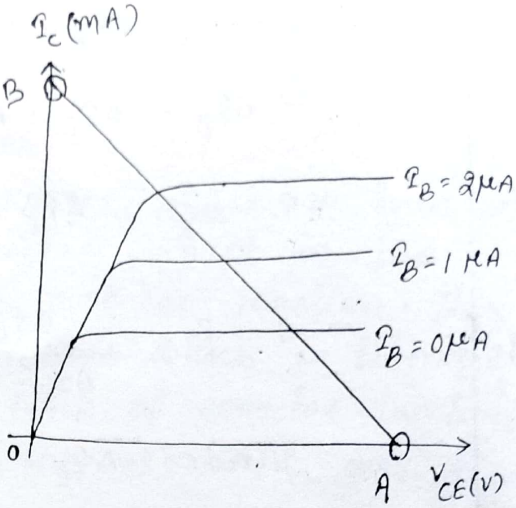
$\Rightarrow r = \frac{\Delta I_E/\Delta I_E}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{1}{1-\alpha}$ //

44. what is active region & cutoff & saturation point of a transistor ?

Sol^{n} :- A. cutoff Point :-

The point where load line intersects $I_B = 0$ curve is known as cutoff point. At this point both emitter - base & collector - emitter regions are reverse bias.

So, $V_{CE(off)} = V_{CC}$



B. Saturation :-

The point where the load line intersects $I_B = I_{B(sat)}$ curve is known as saturation point. At this point, both emitter - base & collector - emitter regions are forward bias.

So, $I_{C(sat)} = \frac{V_{CC}}{R_C}$

C. Active regions :-

The regions between cutoff & saturation, is known as active regions. At this point, emitter - base junⁿ is forward biased & collector - emitter junⁿ is reverse biased. //

45. what is stabilisation & stability factor ?

Sol^{n} :-

A. Stabilisation :-

The process of making operating point independent of temp. changes or variations in transistor parameters is known as stabilization.

B. Stability Factor :-

The rate of change of collector current w.r.t the collector leakage current I_{CBO} at constant β & I_B, is called stability factor.

$$\Rightarrow S = \left.\frac{dI_C}{dI_{CBO}}\right|_{\beta \text{ \& } I_B = \text{constant}}$$

//

46. Why transistor is a current-controlled device?

Sol^{n}:- The output voltage, current or power is controlled by the input current in a transistor so, it is current controlled device. //

47. Why is the width of base region of a transistor is kept very small as compared to other regions?

Sol^{n}:- Base region of a transistor is kept very small & very lightly doped so as to pass most of the injected charge carriers to the collector. //

48. Why silicon type transistors are more often used than germanium type?

Sol^{n}:- Because Silicon has smaller cutoff point I_{CBO}, small variation in I_{CBO} due to variation in temp. & high operating temp. as compared to those in case of germanium. //

49. Why there is maximum limit of collector supply voltage for a transistor?

Sol^{n}:- Although collector current is partially independent of collector supply voltage over the transistor operating range, but if V_{CB} is increased beyond a certain value of collector current I_C eventually increases rapidly & possible distroys the device. //

50. Why common-collector configuration seldom used?

Sol^{n}:- common-collector configuration is seldom used because its voltage gain is always less than unity. //

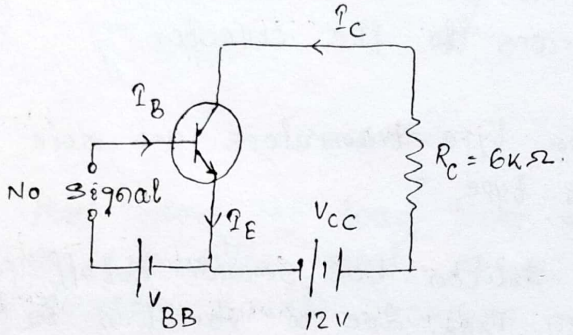
51. What is Early effect?

Sol^{n}:- The modulation of effective base width by the collector voltage is known as modulation of early effect. An increase in collector voltage, increases the space charge width at the output junⁿ diode & thus the effective base width is reduced. //

52. Explain why ordinary transistor is bipolar ?

Sol^n:- Because the transistor operation is carried out by two charge carriers (majority (electrons) & minority (holes)), an ordinary transistor is called bipolar.

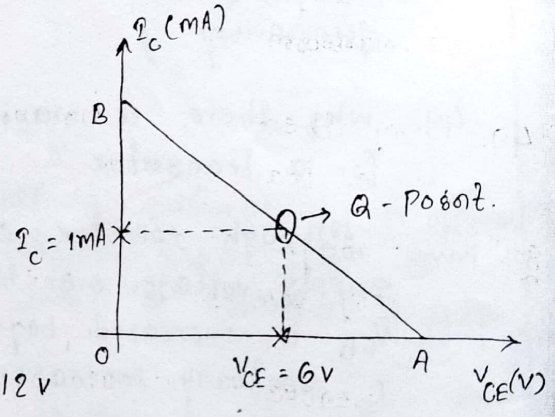
53. In the ckt. diagram, if $V_{CC} = 12\,V$ & $R_C = 6\,K\Omega$, draw the d.c. load line. What will be the Q-point if zero signal base current is $20\,\mu A$ & $\beta = 50$?



Sol^n:- Given. $V_{CC} = 12\,V$

$R_C = 6\,K\Omega$

$I_B = 20\,\mu A$, $\beta = 50$



Apply KVL at o/p, get,

$$V_{CE} = V_{CC} - I_C R_C$$

(i) when $I_C = 0$, $V_{CE} = V_{CC} = 12\,V$

(ii) when $V_{CE} = 0$, $I_C = V_{CC}/R_C = \frac{12\,V}{6\,K\Omega} = 2\,mA$

for Q-point;

$$I_C = \beta I_B = 50 \times 20\,\mu A = 50 \times 0.02\,mA$$

$$= 1\,mA$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 12\,V - 1mA \times 6\,K\Omega = 12 - 6 = 6\,V.$$

54. The value β for a transistor is 100. If the value of emitter current is 10 mA, then value collector & base current is how much ?

Sol^{n}:- Given. $\beta = 100$

$I_E = 10\,mA$

we know,

$$\beta = \frac{\alpha}{1-\alpha}$$

$$\Rightarrow (1-\alpha)\beta = \alpha$$

$$\Rightarrow \beta - \alpha\beta = \alpha$$

$$\Rightarrow \alpha = \frac{\beta}{\beta+1} = \frac{100}{101} = 0.98$$

$$\alpha = \frac{I_C}{I_E}$$

$$\Rightarrow I_C = \alpha I_E = 0.98 \times 10\,mA$$

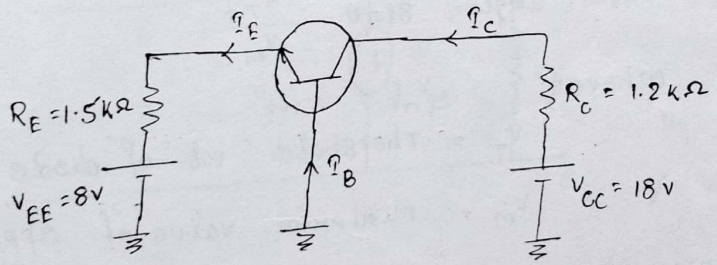
$$= 9.8\,mA.$$

& $I_E = I_B + I_C$

$$\Rightarrow I_B = I_E - I_C = 10\,mA - 9.8\,mA$$

$$= 0.2\,mA. \;//$$

55. For a common-base circuit shown in fig., determine I_C & V_{CB}. As the transistor to be silicon?



Sol^{n}:- Apply KVL at i/p, we get,

$$V_{BE} + I_E R_E - V_{EE} = 0$$

$$\Rightarrow I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{8 - 0.7}{1.5}$$

$$= 4.87\,mA \approx I_C$$

Apply KVL at o/p, we get,

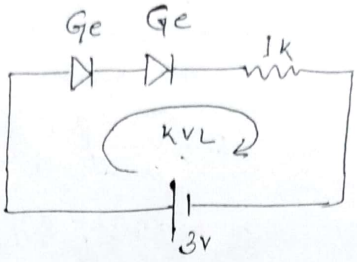
$$V_{CC} - I_C R_C - V_{CB} = 0$$

$$\Rightarrow V_{BC} = V_{CC} - I_C R_C = 18 - (4.87 \times 1.2)$$

$$= 12.16\,V. \;//$$

56. Draw the load line for the following ckt. Is a d.c. load line or a.c. load line ?

Sol^n :-



Apply KVL, we get,

$$3V - V_D - V_D - I_D \times 1K = 0$$

$$\Rightarrow 3V - 2V_D - I_D = 0$$

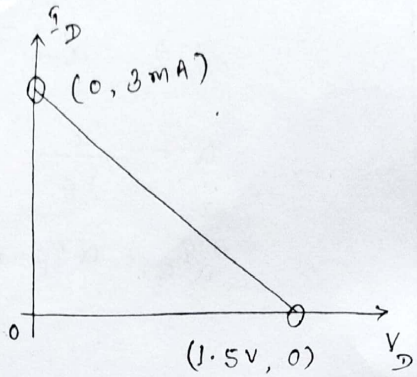
$$\Rightarrow 2V_D = 3 - I_D \longrightarrow (1)$$

When $V_D = 0$

$$\Rightarrow I_D = 3\ mA$$

When $I_D = 0$

$$\Rightarrow V_D = 3/2 = 1.5\ V$$



//

57. In a certain Si rectifier circuit, the cut in angle is 40°. Find out the minimum value of the applied voltage for this angle to occur ?

Sol^n :- The minimum value of applied voltage for cut in angle to occur is 0.7 V.

$$\text{Cut in angle, } \sin\theta = \frac{V_T}{V_m}$$

where;

V_T = Thershold vol. of diode = 0.7 V

V_m = minimum value of applied vol.

$$\Rightarrow \sin\theta = \frac{0.7}{V_m}$$

$$\Rightarrow V_m = \frac{0.7}{\sin\theta} = \frac{0.7}{\sin 40^\circ} = 1.09\ V.$$ //

58. What do you mean by the small signal analysis of BJT ?

Sol^n :- It is an analysis which permitting the use of superposition theorem to isolate the d.c. analysis from the a.c. analysis.

Transistor small signal amplifiers can be considered linear for most application. //

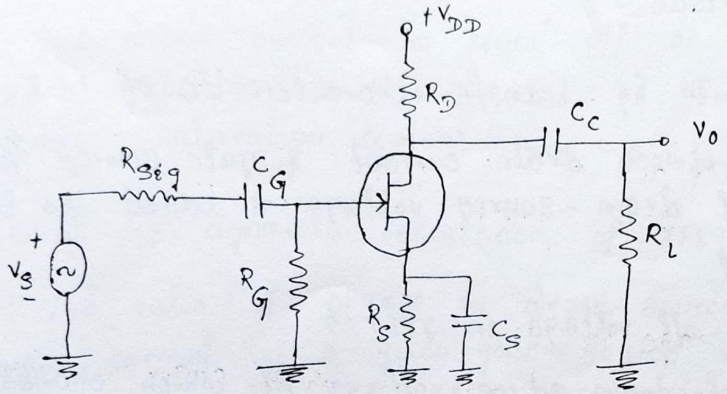
59. Which of the following methods can be used for the biasing of depletion type of MOSFETS :

(i) Gate bias (ii) self-bias (iii) voltage divider bias (iv) current source bias ?

Sol^n :- self-bias & voltage divider bias methods can be used for biasing of depletion type of MOSFET. //

60. Draw the equivalent circuit model of an FET in common source configuration at low frequencies ?

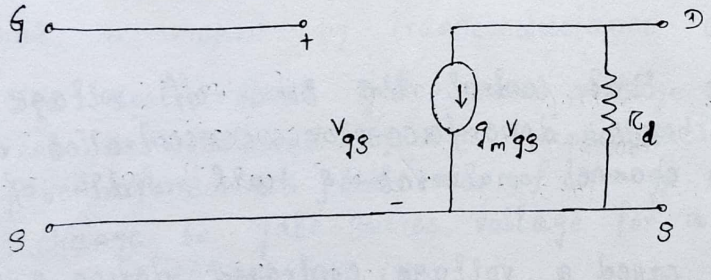
Sol^n :-



//

61. Give the low frequency equivalent circuit of an FET ?

Sol^n :-



//

62. Why are field-effect transistor is called unipolar transistor ?

Sol^n :- In field-effect transistors current conduction is done by only one type of majority carriers (either by electrons or by holes) & therefore, these are called unipolar transistors. //

63. Why the channel of a JFET is never completely closed at the drain end ?

Sol^n :- If the channel is completely closed in JFET, then there will be no drain current, so there will be no voltage drop along the channel length & amount of reverse bias will

become uniform & wedge-shaped depletion region will become rectangular one. //

64. How is drain current controlled in JFET ?

Sol^n:- In JFET drain current is controlled by controlling the reverse bias given to its gate (i.e. V_{GS}). //

65. What is meant by drain characteristic of FET ?

Sol^n:- The curve between drain current & drain-source voltage with gate-to-source voltage as the parameter is called the drain characteristic. //

66. What is meant by transfer characteristic of FET ?

Sol^n:- The curve between drain current & gate-source voltage for a given value of drain-source voltage is called the transfer characteristic. //

67. What is pinch-off voltage in JFET ?

Sol^n:- The value of drain-source voltage at which channel is pinched off (i.e. all the free charges from the channel get removed) is called the pinch-off voltage. //

68. What are the parameters that control the pinch-off voltage of JFET ?

Sol^n:- Parameters that control the pinch-off voltage of JFET are electron charge, donor/acceptor concentration density, permitivity of channel material & half width of channel bar. //

69. Why FET is called a voltage controlled device ?

Sol^n:- In a FET, drain current is controlled by the effect of the extension of the field associated with the depletion region developed by the reverse bias on the gate, so it is called a voltage controlled device. //

70. How does the current vary with the gate voltage in the saturation region ?

Sol^n:- The drain current decrease with increase in gate-source bias $|V_{DS}|$. when $V_{GS} = 0$, drain current $I_D = I_{DSS}$, drain source saturation current & when $V_{GS} = V_P$, drain current $I_D = 0$. //

71. what is meant by gate-source cutoff voltage ?

Sol^n :- The gate source bias voltage required to reduce the drain current to zero is designated the gate-source cutoff voltage $V_{GS(off)}$. It is equal to pinch-off voltage V_P. //

72. What is meant by saturation region ?

Sol^n :- The region of drain characteristic of a FET in which drain current remains fairly constant is called the saturation or pinch-off region. //

73. What is meant by drain-source saturation current I_{DSS} ?

Sol^n :- The drain current in pinch-off or saturation region with zero gate-source voltage ($V_{GS} = 0$) is referred to the drain-source saturation current I_{DSS}. //

74. What is dynamic resistance of JFET ?

Sol^n :- The ratio of change in drain-source voltage to change in drain current at a given gate-source voltage is known as ac drain resistance or dynamic resistance r_d.

$$\Rightarrow r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS} = \text{constant}} //$$

75. what is meant by transconductance with reference to JFET ?

Sol^n :- The control that gate-source voltage has over the drain current is measured by the transconductance of a JFET. It may be defined as the ratio of change in drain current to the change in gate-source voltage for a given value of drain-source voltage i.e.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS} //$$

76. What is the significant difference between the construction of an enhancement type MOSFET & a depletion type MOSFET ?

Sol^n :- In the depletion-type MOSFET a channel is physically constructed & a current between drain & source is due to voltage applied across the drain-source terminals while in enhancement type construction no channel is formed during its construction. voltage is applied to the gate in case of enhancement type MOSFET, to develop a channel of

charge carriers so that a current results when a voltage is applied across the drain-source terminals. //

77. What is the difference between voltage & current feedback?

Sol^{n}:- voltage feedback refers to connecting the output voltage as input the feedback network while current feedback refers to tapping off some output current through the feedback network. //

78. How do series feedback & shunt feedback differ from each other?

Sol^{n}:- series feedback means connecting the feedback signal in series with input voltage while shunt feedback means connecting the feedback signal in parallel with an input current source. //

79. What is the effect of a negative feedback on the input & output impedance of a voltage-series feedback amplifier?

Sol^{n}:- series voltage negative feedback increases the input impedance & reduces the output impedance by a factor $(1+A\beta)$, where $A\beta$ is the feedback factor. //

80. What is the effect of a negative feedback on the bandwidth of an amplifier?

Sol^{n}:- Bandwidth of an amplifier is increased, when negative feedback is introduced, by a factor $(1+A\beta)$ by which its gain is reduced. //

81. What is an oscillator?

Sol^{n}:- oscillator may be defined as the circuit which generates an ac signal of very high frequency without requiring any externally applied input signal or it may be defined as an electronic source of alternating current (or voltage) having sinusoidal or non-sinusoidal (square, sawtooth, or pulse) waveshape. It can also be defined as a circuit that converts dc energy into very high frequency ac energy. //

82. What are the Barkhausen criteria conditions of oscillators?

Sol^{n}:- 1. The loop gain of the circuit must be ≥ 1.

2. The phase shift around the circuit must be zero. //

83. How does a signal generator differ from an ordinary oscillator ?

Sol^{n} :- The signal generator, like an ordinary oscillator, is a source of sinusoidal signals but it is also capable of modulating its sinusoidal output signal with other signals. //

84. What is an operational Amplifier ?

Sol^{n} :- An OP-amp is a very high gain differential amplifier with high input impedance & low output impedance. An OP-amp which can perform arithmatic & logical operations. //

85. State assumptions made for analysing ideal OP-amp ?

Sol^{n} :-
1. High input impedance.
2. output resistance is zero.
3. Differential gain is infinity.
4. If zero signal applied to OP-amp there is no output signal.
5. common mode rejection ratio is infinite.
6. slew rate is infinite. //

86. Define CMRR ?

Sol^{n} :- It is defined as the ratio between the differential gain to common-mode gain.

$$\therefore CMRR = \frac{A_d}{A_c}$$

where, A_d = Differential gain.

A_c = common-mode gain. //

87. Define slew rate ?

Sol^{n} :- It is defined as the maximum rate at which amplifier output can change in volts / microsecond (μs)

$$\Rightarrow \text{slew Rate} = \frac{\Delta V_o}{\Delta t} \quad V/\mu s. \text{ //}$$

88. Why open-loop application ?

Sol^n :- When an open-loop configuration is operated, the output either goes to positive or negative saturation levels or switches between positive & negative saturation levels & thus clips the output above these levels. //

89. Why voltage follower circuit is an ideal device to serve as a buffer amplifier ?

Sol^n :- voltage follower, because of its three unique characteristics of extremely high input impedance, unity transmission gain, extremely low output impedance, is an ideal device to serve as a buffer amplifier. //

90. What is voltage buffer ?

Sol^n :- voltage buffer is an electronic circuit in which output voltage tracks the input voltage both in sign & magnitude. //

91. What are the advantages of using a voltage buffer amplifier ?

Sol^n :- Same as Q. No - (89). //

92. What are the application of inverting amplifier ?

Sol^n :- Inverting amplifier is a very versatile component & can be used for performing number of mathematical simulation such as analog inverter, Paraphase amplifier, phase shifter, adder, integrator & differentiator. //

93. What is differential amplifier ?

Sol^n :- Differential amp. is a combination of inverting & non-inverting amplifier & amplifies the voltage difference between two input lines either of which is grounded. //

94. OP-amp is used mostly as an integrator than a differentiator ?

Sol^n :- OP-amp is mostly used as an integrator rather than a differentiator because in differentiator at high freq gain is high & so high gain noise is also amplified which

absolutely abstract the differentiated signal. //

95. Where does the starting voltage for an oscillator come from ?

Sol^n :- The oscillator is a device which generates sinusoidal signal by using a dc source. Dc source applied maintain a proper flow of current through the oscillator. But the internal noise signal associated with the oscillator device builds up a steady state oscillation condition. //

96. The first stage of an op-amp is a differential amplifier. what is the advantage of this ?

Sol^n :- Whenever is a differential amplifier is taken due to its high input impedance $v_i = 0$ & the total source signal is applied across the input of the device without any load. Again, if $v_i = 0$. the gain $A_v = v_o/v_i = \infty$ i.e. very high. Due to above basic reasons differential amplifier is used at the first stage of an op-amp. //

97. How do you make the gain of an operational amplifier finite ? Justify.

Sol^n :- The gain of an operational amplifier can be made finite by using a feedback connection. //

98. what type of feedback a sinusoidal oscillator uses ? why ?

Sol^n :- A sinusoidal oscillator used positive feedback.
By using positive feedback,

$$A_f = \frac{A}{1 - A\beta}$$

where, A = open-loop gain.

A_f = Gain with feedback.

$1 - A\beta$ = Closed-loop gain.

Now, if it will make $A\beta = 1$. then

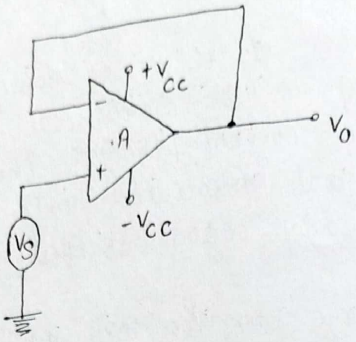
$$A_f = \frac{A}{0} \Rightarrow \frac{v_o}{v_s} = \infty$$

$\Rightarrow v_s = 0$

i.e. we will get output without applying input signal. //

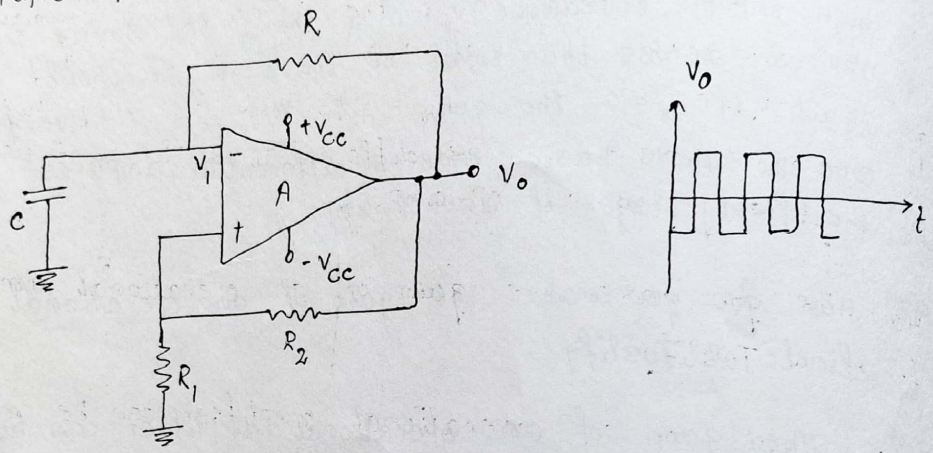
99. Draw the circuit diagram of voltage follower using an operational amplifier ?

Sol^n:-

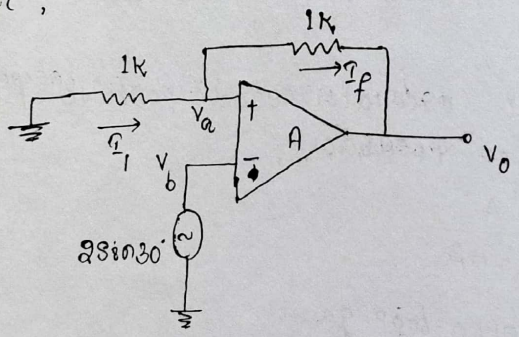


100. Draw a square wave generator using an operational amplifier ?

Sol^n:-



101. Draw the output waveform, to scale of the following circuit;



Sol^n:- In the fig.

$$V_a = V_b = 2\sin 30^\circ$$

Here, $I_1 = \frac{0 - V_a}{R_1} = \frac{0 - 2\sin 30^\circ}{1K}$

$$= -\frac{2\sin 30^\circ}{1K}$$

$$\& \quad I_f = \frac{V_a - V_o}{R_f}$$

$$\Rightarrow I_f = \frac{2\sin 30^\circ - V_o}{1K}$$

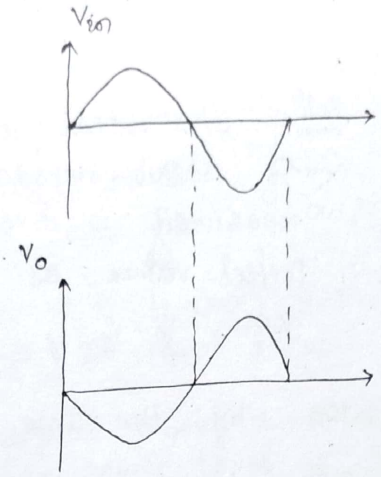
Apply KCL at point 1;

$$\Rightarrow I_1 - I_f = 0$$

$$\Rightarrow I_1 = I_f$$

So, $$\frac{-2\sin 30^\circ}{1K} = \frac{2\sin 30^\circ - V_o}{1K}$$

$$\Rightarrow V_o = -4\sin 30^\circ \quad //$$



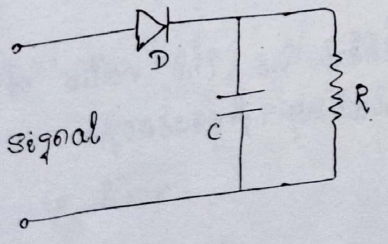
102. How BJT can be used as a switch ?

Sol^n:- When Q point situated at cut off & saturation point, means when Q point is at saturation point at that time both emitter - base jun^n & collector - base jun^n of transistor are forward bias resulting max^m current. So, that transistor will operate as 'ON' switch.

Similarly, when Q point is at cut off point at that time both junction becomes reverse bias so that transistor will operate as 'OFF' switch. //

103. What is the simple circuit used for demodulation of AM signal ?

Sol^n:- The simple circuit used for demodulation of AM signal is diode detector or envelope detector.



//

104. What is the circuit responsible for displaying analog voltage in a digital multimeter ?

Sol^n:- The circuit responsible for displaying analog voltage in a digital multimeter is analog to digital converter. //

105. what should be the ideal input impedance of a voltmeter? why?

Sol^n:- The ideal input impedance of a voltmeter is infinite. If input impedance will very high. The voltage to be measured is directly applied to the meter & will get the perfect value, as input current is zero & also voltage is zero.

Hence, $V_0 = V_s$ //

106. why the time base in a CRO is of saw-tooth type?

Sol^n:- The sawtooth nature of horizontal time base drives the applied input voltage at a constant rate.

It provides the necessary left to right horizontal deflection for the verified signal so that proper viewing is possible. //

107. what are FM modulation & AM modulation index?

Sol^n:- AM modulation index :-

The ratio of change in carrier amplitude to the original carrier amplitude is called modulation index or depth of modulation.

$$\text{So, } m_a = \frac{E_m}{E_c}$$

where, E_m = max^m amplitude of base-band signal.

E_c = max^m amplitude of carrier signal.

$$\text{So, } m_a = \frac{E_{max} - E_{min}}{E_{max} + E_{min}}.$$

FM modulation index :-

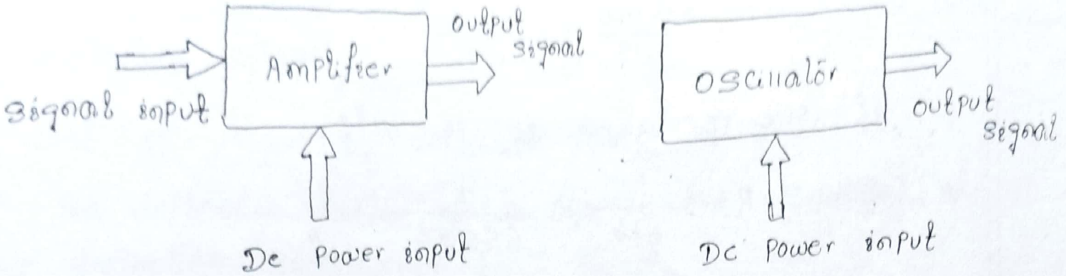
It is defined as the ratio of change in carrier frequency to the modulating frequency.

$$\Rightarrow \beta = \frac{\Delta f}{f_m}$$

$$= \frac{\text{change in freq w.r.t carrier freq}}{\text{modulating freq}}$$ //

108. Give the comparison between an amplifier & an oscillator?

Sol^n:-



An amplifier produces an output signal whose waveform is similar to the input signal but whose power level is generally high. The additional power is provided by the external d.c. source. Hence, an amplifier is essentially an energy converter i.e. it takes energy from d.c. source & converts it into ac energy at signal frequency. The process of energy conversion is controlled by the input signal. If there is no input signal, there is no energy conversion & there is no output signal.

The oscillator does not need an external signal either to start or maintain energy conversion process. It keeps producing an output signal so long as the dc power source is connected. //

109. Why the time-base in a CRO is of saw-tooth type?

Sol^n:- The saw-tooth nature of the horizontal time-base drives the applied input voltage at a constant rate. It provides the necessary left to right horizontal deflection for the verified signal so that proper viewing is possible. //

110. List four timing parameters of a flip-flop?

Sol^n:- 1. Propagation delay of gates used in the flip-flop.
2. Width of clock pulse.
3. set up time.
4. Hold time. //

111. What are the resolution of 12 bits & 16 bits D/A converter?

Sol^n:- Resolution of D/A converter is given by,

$$\Rightarrow R = \frac{1}{2^N}$$

where, N = no. of bits.

If the resolution is 12-bits.

$$\Rightarrow R = \frac{1}{2^{12}} = \frac{1}{4096}.$$

If the resolution is 16-bits.

$$\Rightarrow R = \frac{1}{2^{16}} = \frac{1}{65536}. \quad //$$

112. An amplifier has an input voltage of 8 mv & output voltage of 480 mv. The input current is in phase with voltage is 200 μA, power gain is 3000. Determine (i) voltage gain (ii) output current ?

Sol^n:- Given,

$V_i = 8$ mv

$V_0 = 480$ mv

(i) voltage gain, $A_V = \frac{V_0}{V_i} = \frac{480}{8} = 60$ mv

(ii) Power gain, $\frac{P_0}{P_i} = 3000$

$$\Rightarrow \frac{V_0 I_0}{V_i I_i} = 3000$$

$$\Rightarrow I_0 = 3000 \times \frac{V_i}{V_0} \times I_i$$

$$= 3000 \times \frac{8}{480} \times 0.2\,mA$$

$$= 10\,mA. \quad //$$

113. For what a triggering circuit is provided in a CRO ?

Sol^n:- In a CRO, a triggering circuit is provided for synchronising two types of deflections so that horizontal deflection starts at the same point of the input vertical signal each time it sweeps. //

114. For what electron gun assembly is provided in a CRT ?

Sol^n:- The sole function of an electron gun assembly in a CRO is to provide a narrow & sharply focused electron beam which is accelarated towards the phosphor screen. //

115. What is meant by deflection sensitivity of a CRO?

Sol^n:- The deflection sensitivity of a CRO is defined as the vertical deflection of the beam on the screen per unit deflecting voltage. //

116. What is meant by deflection factor of a CRO?

Sol^n:- The deflection factor of a CRO is the reciprocal of the deflection sensitivity. //

117. ~~Name~~ two applications of a CRO?

Sol^n:- Measurement of phase difference & frequency of a voltage signal. //

118. What is time base of a CRO?

Sol^n:- (i) The spot moves from left to right over the same path again for every ~~of~~ cycle of saw-tooth voltage applied to the horizontal deflection plates, so a horizontal line appears on the screen of CRO.

(ii) The spot moves from left to right on the screen with the uniform speed. Thus it produces a linear time base to display function of time on the screen of CRO. //

119. What are the advantages & disadvantages of crystal oscillator?

Sol^n:- Advantages :-

1. It is very simple circuit as it does not need any tank circuit other than crystal itself.
2. Different oscillation freq can be had by simple replacing one crystal with another.
3. The Q-factor, which is measure of the quality of resonance circuit of a crystal, is very high. The Q-factor of a crystal may range from 10^4 to 10^6 whereas the LC circuit may have a Q-factor only of the order of 100. //

Disadvantages :-

1. The crystal oscillator have a very limited tuning range. They are ~~not~~ used for freq exceeding 100 KHz.
2. The crystal oscillators are fragile &, therefore, can only be used in low power circuits. //

120. what are the ... shift oscillator ?

Sol^n :- Advantages :-

1. It is cheap & simple circuit as it contains resistors & capacitors.
2. It provides good freⁿ stability.
3. The output is sinusoidal that is quite distortion free.
4. They have very wide range of freⁿ (from few Hz to seve KHz).
5. The phase-shift oscillator circuit is much simpler than the wien bridge oscillator circuit because it does not need negative feedback.

Disadvantages :-

1. The output is small. It is due to smaller feedback.
2. It is difficult for the circuit to start oscillatoons as the feedback is usually small.
3. The freⁿ stability is not as good as that of wein bridge oscillator. //

121. find the modulation index in an AM system where m(t) is $\sin 200\pi t$ & c(t) is $4\sin 2000\pi t$?

Sol^n :-

Given,

$$m(t) = \sin 200\pi t$$

$\because A_m = 1$

& $c(t) = 4\sin 2000\pi t$

$\because A_c = 4$

Now, mod^n index $\Rightarrow m = \frac{A_m}{A_c} \times 100$

$$= \frac{1}{4} \times 100 = 25\%$$

//

122. A Lissajous Pattern on a CRO has 5 horizontal tangencies & 2 vertical tangencies. The freⁿ of horizontal input is 1 KHz. What is the freⁿ of the vertical input?

Given, $\frac{f_h}{f_v} = \frac{5}{2}$

$\therefore$ f_h = freq of horizontal input.

f_v = freq of vertical input.

& $f_h = 1$ KHz

So, $\frac{f_h}{f_v} = \frac{5}{2}$

$\Rightarrow f_v = \frac{2 \times f_h}{5} = \frac{2 \times 1}{5} = 0.4$ KHz. //

123. List four timing parameters of a flip-flop ?

Sol^n:- 1. Propagation delay of gates used in the flip-flop.

2. width of clock pulse.

3. set up time.

4. Hold time. //

124. The output voltages of an amplifier with 10 V at 5 KHz & 7.07 V at 25 KHz. what is the decibel change in the output power level ?

Sol^n:- Given,

O/p voltage $\Rightarrow V_o = 10$ V

I/p voltage $\Rightarrow V_i = 7.07$ V

Power level $= 20 \log_{10} \frac{V_o}{V_i}$

$= 20 \log_{10} \frac{10}{7.07} = 3$ db. //

125. A three stage amplifier has first stage voltage gain of 100, 200 for 2nd stage, 3rd stage voltage gain of 400. Find the total voltage gain in db ?

Sol^n:- In Multistage amp., voltage gain $= 20 \log_{10}(A_1 A_2 A_3)$

$= 20 \log_{10} (100 \times 200 \times 300)$

$= 138$ db. //

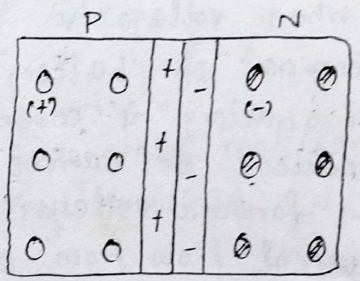
LONG QUESTIONS

1. Distinguish between majority & minority carriers. Explain the formation of depletion layer in a PN-junction ?

Sol^{n}:- The N-type material has large no. of free electrons where as P-type material has large no. of holes. At room temp., some of co-velent bond breaks & thus gives equal no. of free electrons & holes but more no. of electrons are present due to effect of impurity. So, N-type material has electrons are the majority carrier & holes are minority carrier.

Similarly, P-type material has holes are majority carrier & free electrons are minority carrier.

Formation of Depletion Layer :-

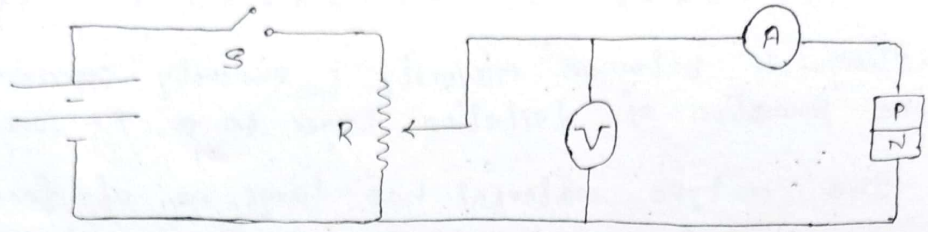


The process of diffusion takes place for sometimes & then stops. Because of electrostatic induction the continous entry of -ve charge electrons to the P-type creates a -ve layer beside the junⁿ. Similarly, the continous entry of +ve charge holes to the N-type creates a layer of +ve charge beside the junⁿ.

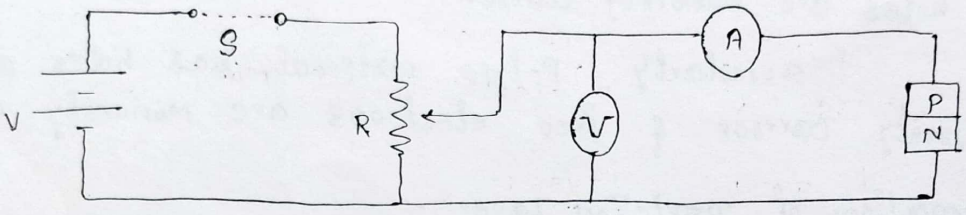
Now, when electron will try to jump to the P-type, the -ve charge layer will repal it back, And holes will jump to the N-type, the +ve layer will repal it back. Hence, the barrier is establish near the junⁿ which prevents the process of diffusion. That barrier is called potential barrier. The region occupied by potential barrier is known as depletion layer.

2. Explain the V-I characteristic of PN-Junction diode? Is this diode a linear device?

Sol^{n}:-



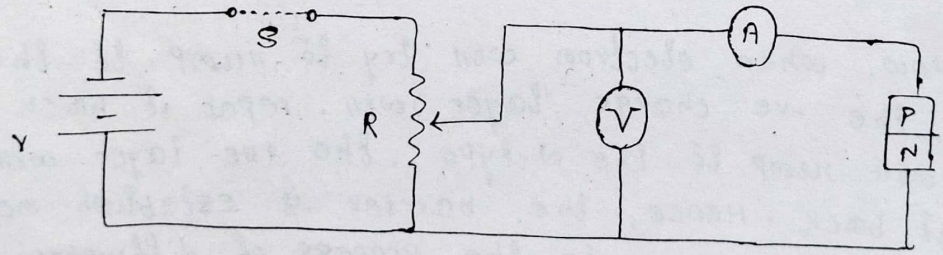
→ When an external voltage is zero, the circuit is open & the potential barrier at diode does not permit the current flow. The current is zero at point 'O'.



→ When voltage 'V' is applied, switch is closed i.e. +ve terminal of battery is connected to P-type & -ve terminal of battery is connected to N-type, the potential barrier is reduced. So, current flowing in the circuit & it increase in forward voltage. In V-I characteristic of diode, the current flow from O to A very slowly & the curve is non-linear. After A, the current raises very sharply with increase in external voltage.

3.

Sol^{n}

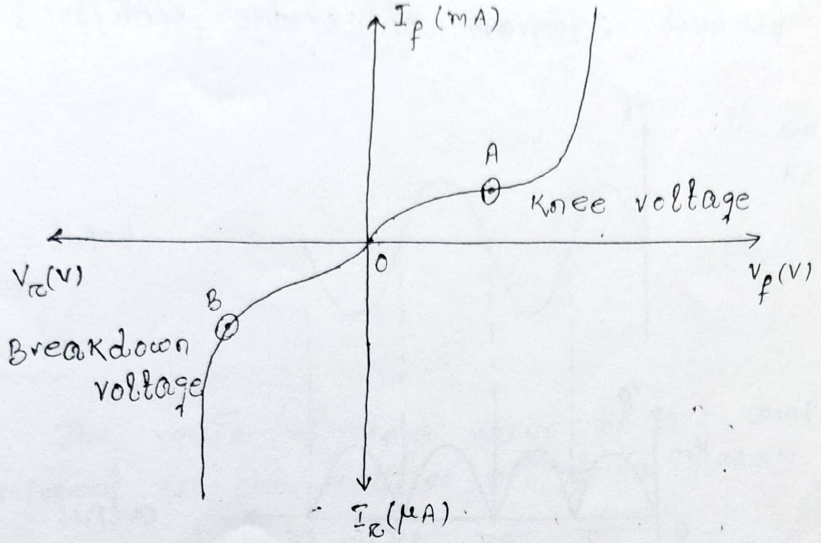


→ When voltage is reversed, switch is closed i.e. -ve terminal of battery is connected to P-type & +ve terminal of battery is connected to N-type, the potential barrier of diode is increased. So, no current flow through the circuit.

But if reverse bias is increased, the K.E. of minority carriers (i.e. electrons in P & holes in N) is

increased, as a result very small amount of current (μA) flows in reverse biased.

If reverse voltage is increase further, K.E. of minority carrier high such that junⁿ may breakdown. This may distroyed the junⁿ permanantly. This phenomenon is known as avalanche breakdown.



V-I characteristic of diode

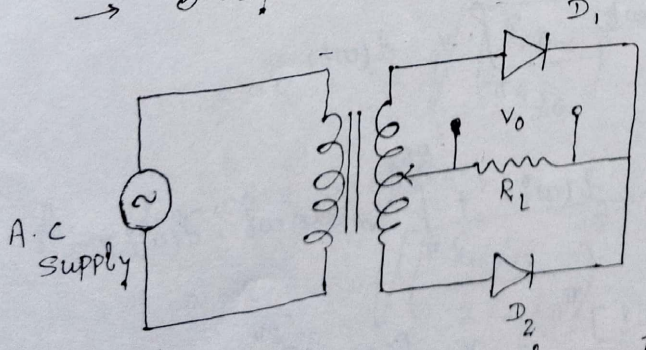
3. Draw the circuit diagram of full-wave rectifier & derive the expression for d.c. output voltage, d.c. output current, & ripple factor?

Solⁿ:- In full-wave rectifier, current flows through the load in same dirⁿ for both half-cycle of input a.c. voltage.

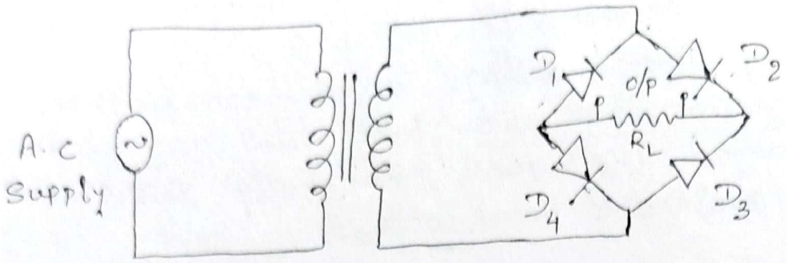
For +ve half-cycle of input voltage one diode supplies current to load & for -ve half-cycle other diode does so.

→ centretapped rectifier.

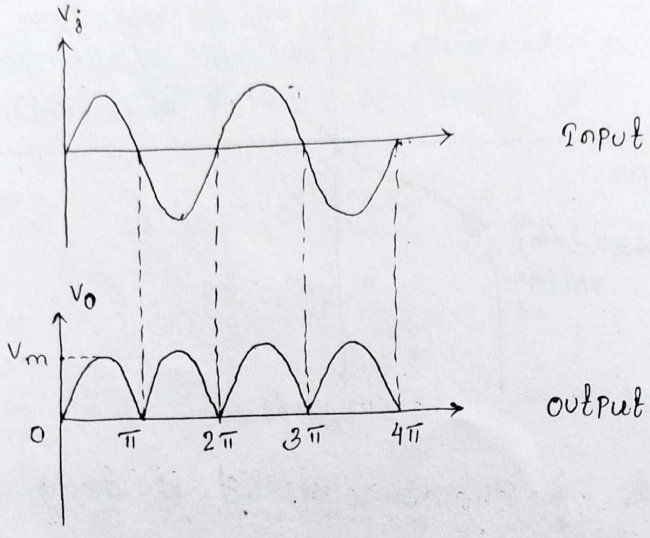
→ Bridge rectifier.



(Circuit Diagram of centretapped rectifier)



(Circuit Diagram of Bridge rectifier)



From the output waveform,

$V_o = V_m \sin \omega t, \quad 0 \le \omega t \le \pi$

$V_o = -V_m \sin \omega t, \quad \pi \le \omega t \le 2\pi$ (-ve sign indicate that the sine wave is inverted)

$$V_{dc} = \frac{\text{Area under the curve over full-cycle}}{\text{Base}}$$

$$\text{Area} = \int_0^{2\pi} V_o \cdot d(\omega t)$$

$$= \int_0^{\pi} V_o \cdot d(\omega t) + \int_{\pi}^{2\pi} V_o \cdot d(\omega t)$$

$$= \int_0^{\pi} V_m \sin \omega t \cdot d(\omega t) + \int_{\pi}^{2\pi} -V_m \sin \omega t \cdot d(\omega t)$$

$$= V_m [-\cos \omega t]_0^{\pi} + V_m [\cos \omega t]_{\pi}^{2\pi}$$

$$= V_m[-\cos\pi - (-\cos 0)] + V_m[\cos 2\pi - \cos\pi]$$

$$= V_m[1+1] + V_m[1+1] = 4V_m$$

$$V_{dc} = \frac{4V_m}{2\pi} = \frac{2V_m}{\pi}$$

$$\left\{ I_{dc} = \frac{V_{dc}}{R_L} = \frac{2V_m}{\pi R_L} = \frac{2I_m}{\pi} \right. \quad \left(\because I_m = \frac{V_m}{r_f + R_L} \right.$$

If diode is ideal,

$r_f = 0$

so, $I_m = \frac{V_m}{R_L}$)

Ripple factor :-

The ratio of rms value of a.c. component to the d.c. component in the rectifier output is known as ripple factor.

$$\Rightarrow R.F. = \frac{I_{ac}}{I_{dc}}$$

By defination,

$$I_{rms} = \sqrt{I_{ac}^2 + I_{dc}^2}$$

$$\Rightarrow I_{rms}^2 = I_{ac}^2 + I_{dc}^2$$

$$\Rightarrow I_{ac}^2 = I_{rms}^2 - I_{dc}^2$$

$$\Rightarrow I_{ac} = \sqrt{I_{rms}^2 - I_{dc}^2}$$

Divide I_{dc} on both sides, we get :

$$\Rightarrow \frac{I_{ac}}{I_{dc}} = \frac{1}{I_{dc}} \sqrt{I_{rms}^2 - I_{dc}^2}$$

$$\Rightarrow R.F. = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} \longrightarrow (1)$$

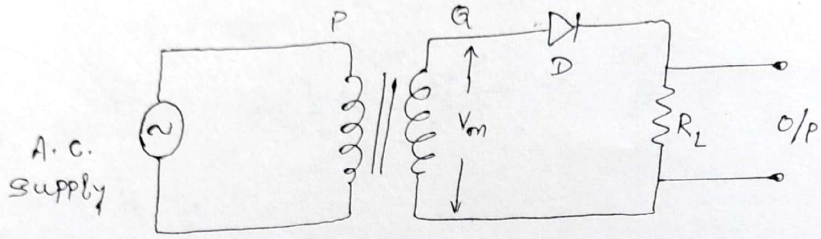
for full-wave rectifier,

$$\Rightarrow R.F. = \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1}$$

$$= 0.482$$

4. Explain the working function of Half-wave rectifier?

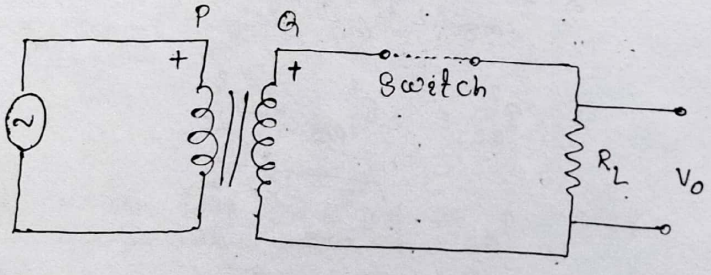
Sol^n:- The half-wave rectifier is a device which rectifies only one half of signal & block the other.



(Ckt diagram)

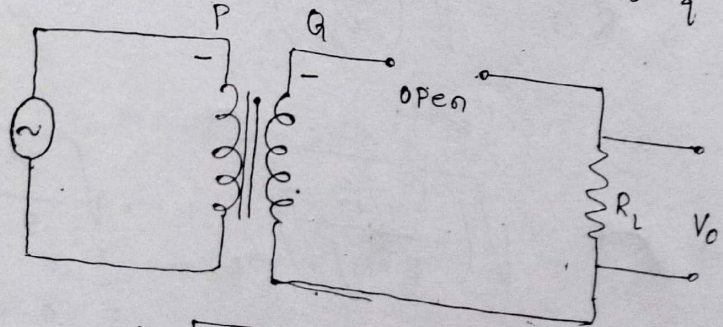
→ The circuit consist of a step-down transformer to which a.c. input is applied. To the secondary winding of transformer a crystal diode is connected. A diode resistance R_L is connected in series with the diode across which d.c. o/p is obtain.

→ When a.c. voltage is fed to the primary winding of transformer, the voltage is transferred to the secondary winding. When +ve half-cycle is passed through crystal diode, the arrowhead of diode becomes +ve with respect to bar. Hence, diode behaves as forward biased & short circuit.



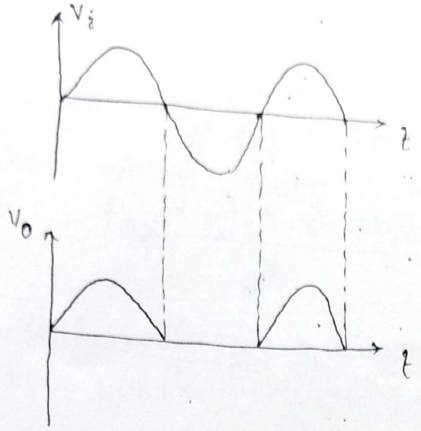
$\Rightarrow \boxed{V_o = V_{in}}$

→ When -ve half-cycle is passed through crystal diode, the arrowhead of diode becomes -ve with respect to bar. Hence, diode behaves as reverse biased & open circuit.



$\Rightarrow \boxed{V_o = 0V}$

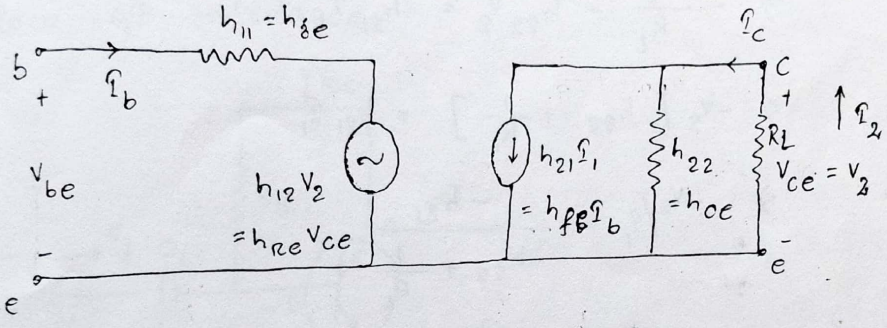
→ The wave-form is,



//

5. Find the expression for current gain, voltage gain of the CE configuration from the small-signal hybrid model.

Sol^n:-



From hybrid-model the eqn^n are,

$$V_1 = h_{11} I_1 + h_{12} V_2$$

$$I_2 = h_{21} I_1 + h_{22} V_2$$

current gain, $A_i = \dfrac{I_2}{I_1}$

$$\therefore I_2 = h_{21} I_1 + h_{22} V_2$$

$$= h_{21} I_1 - h_{22} I_2 R_L \qquad (\because V_2 = -I_2 R_L)$$

$$\Rightarrow I_2 + h_{22} I_2 R_L = h_{21} I_1$$

$$\Rightarrow I_2 (1 + h_{22} R_L) = h_{21} I_1$$

$$\Rightarrow \frac{I_2}{I_1} = A_i = \frac{h_{21}}{1 + h_{22} R_L} = \frac{h_{fe}}{1 + h_{oe} R_L}$$

Input impedance, $Z_i = \frac{V_1}{I_1}$

$\because V_1 = h_{11} I_1 + h_{12} V_2$.

So, $Z_i = \frac{h_{11} I_1 + h_{12} V_2}{I_1}$

$= h_{11} + h_{12} \frac{V_2}{I_1}$

& $I_2 = h_{21} I_1 + h_{22} V_2$

$\Rightarrow -\frac{V_2}{R_L} = h_{21} I_1 + h_{22} V_2$ $\left(\because V_2 = -I_2 R_L \right.$

$\left. \Rightarrow I_2 = -\frac{V_2}{R_L}\right)$

$\Rightarrow -\frac{V_2}{R_L} - h_{22} V_2 = h_{21} I_1$

$\Rightarrow -V_2 \left[h_{22} + \frac{1}{R_L} \right] = h_{21} I_1$

$\Rightarrow V_2/I_1 = \frac{-h_{21}}{h_{22} + \frac{1}{R_L}}$

& $Z_i = h_{11} + h_{12} \frac{V_2}{I_1}$

$= h_{11} + h_{12} \left[\frac{-h_{21}}{h_{22} + \frac{1}{R_L}} \right]$

$= h_{11} - \frac{h_{12} h_{21}}{h_{22} + \frac{1}{R_L}}$ $= h_{ie} - \frac{h_{re} h_{fe}}{h_{oe} + \frac{1}{R_L}}$.

Voltage gain, $A_V = \frac{V_2}{V_1}$

We know, $Z_{in} = \frac{V_1}{I_1}$

$\Rightarrow V_1 = I_1 \times Z_{in}$

So, $A_V = \frac{V_2}{I_1 \times Z_{in}} = \frac{1}{Z_{in}} \times \frac{V_2}{I_1}$

$= \frac{1}{Z_{in}} \times \frac{-h_{21}}{h_{22} + \frac{1}{R_L}} = \frac{1}{Z_{in}} \times \frac{-h_{fe}}{h_{oe} + \frac{1}{R_L}}$

6. Draw an emitter follower circuit & derive its voltage gain, input impedance & output impedance using r_e model ?

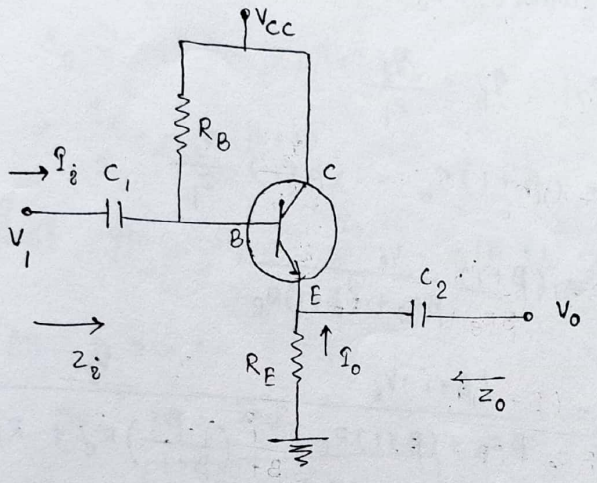
Sol^n:-

→ When the o/p is taken from the emitter terminal of the transistor, the n/w is referred to as an emitter follower.

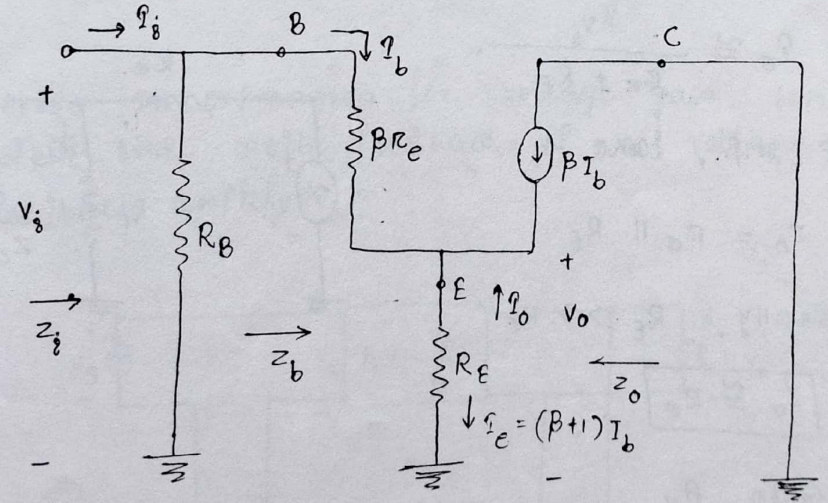
→ The output voltage is always slightly less than the input voltage but a voltage gain, $A_v \cong 1$.

→ The output voltage is in phase with the input. Hence, as the o/p voltage has a magnitude almost equal to that of the input with in phase relationship.

→ Emitter-follower configuration has high i/p impedance but low o/p impedance.



(CKt diagram)



(r_e - Model)

Input impedance, Z_i

$$Z_i = R_B \parallel Z_b$$

$$\because Z_b = \beta r_e + (\beta+1) R_E$$

with $\beta >> 1$

$$\Rightarrow Z_b \cong \beta r_e + \beta R_E \cong \beta (r_e + R_E)$$

$$\Rightarrow \boxed{Z_b \cong \beta R_E}$$

So, $\boxed{Z_i = R_B \parallel \beta R_E}$

Output impedance, Z_o

Now, $I_b = \frac{V_i}{Z_b}$

$$I_e = (\beta+1) I_b = (\beta+1) \frac{V_i}{Z_b}$$

$$= (\beta+1) \frac{V_i}{\beta r_e + (\beta+1) R_E}$$

$$= \frac{(\beta+1) V_i}{\beta r_e + (\beta+1) R_E} = \frac{V_i}{\left(\frac{\beta}{\beta+1}\right) r_e + R_E}$$

But $\beta >> 1$, so,

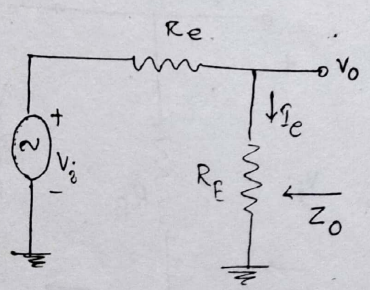
$$I_e \cong \frac{V_i}{r_e + R_E}.$$

For o/p imp., take $V_i = 0$

$\therefore Z_o = r_e \parallel R_E$

usually, $R_E >> r_e$

So, $\boxed{Z_o \cong r_e}$



Voltage Gain, A_v.

According to above fig.,

$$V_o = \frac{R_E \times V_i}{R_E + r_e}$$

$$\Rightarrow \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e} = A_v$$

Usually $R_E >> r_e$

So, $R_E + r_e \cong R_E$

$$\Rightarrow \boxed{A_v \cong \frac{R_E}{R_E} \cong 1}$$

Current gain, A_i,

From r_e - model,

$$I_b = \frac{R_B I_i}{R_B + Z_b}$$

$$\Rightarrow \frac{I_b}{I_i} = \frac{R_B}{R_B + Z_b}$$

& $I_o = -I_e = -(\beta+1) I_b$

$$\Rightarrow \frac{I_o}{I_b} = -(\beta+1)$$

Current gain, $A_i = \frac{I_o}{I_b} = -(\beta+1)\frac{R_B}{R_B + Z_b}$

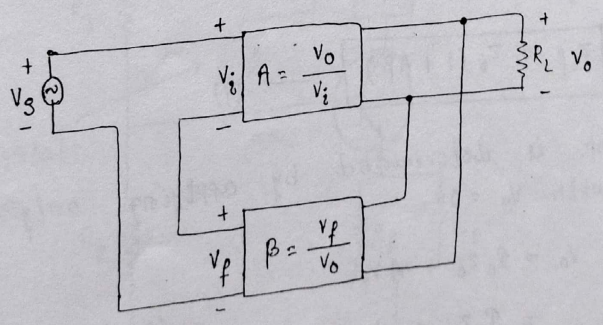
AS $\beta >> 1$

So, $\beta + 1 \cong \beta$

Hence, $\boxed{A_i \cong \frac{-\beta R_B}{R_B + Z_b}}$ //

7. Derive an expression for voltage gain, input imp. & output imp. with feedback of a voltage-series feedback amplifier ?

Soln :-



The above fig. shows the voltage-series feedback connection with a part of output voltage feedback in series with input signal. If there is no feedback voltage, $V_f = 0$

So, Gain $(A) = \frac{V_o}{V_i}$ $\longrightarrow$ (1)

If V_f is connected in series with input, then,

$$V_s = V_i + V_f$$

$$\Rightarrow V_i = V_s - V_f \longrightarrow (2)$$

From eqn (1),

$$V_o = A V_i$$

$$= A(V_s - V_f)$$

$$= AV_s - AV_f = AV_s - A\beta V_o \quad (\because V_f = \beta V_o)$$

$$\Rightarrow V_o + A\beta V_o = AV_s$$

$$\Rightarrow V_o(1 + A\beta) = AV_s$$

$$\Rightarrow \boxed{\frac{V_o}{V_s} = A_{V_f} = \frac{A}{1 + A\beta}} \longrightarrow (3)$$

From eqn (2),

$$V_i = V_s - V_f$$

$$\Rightarrow V_s = V_i + V_f$$

$$= I_i Z_i + \beta V_o = I_i Z_i + \beta A V_i$$

$$= I_i Z_i + A\beta I_i Z_i$$

$$= I_i Z_i (1 + A\beta)$$

$$\Rightarrow \frac{V_s}{I_i} = Z_i (1 + A\beta)$$

$$\Rightarrow \boxed{Z_{if} = Z_i (1 + A\beta)} \longrightarrow (4)$$

The o/p imp. is determined by applying only voltage v, current I with $V_s = 0V$.

So, $V_o = I_o Z_o + A V_i$

$= I_o Z_o + A(-V_f)$ $\quad (\because V_s = V_i + V_f \Rightarrow V_i = -V_f)$

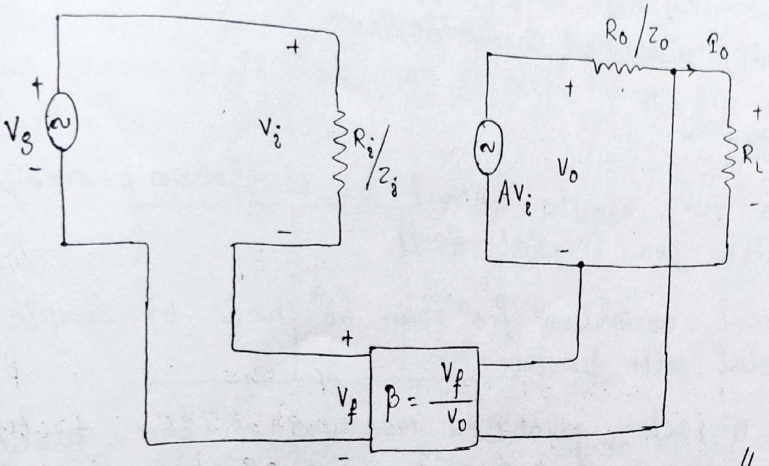
$$V_o = I_o Z_o - A V_f$$

$$= I_o Z_o - A\beta V_o$$

$$\Rightarrow V_o (1 + A\beta) = I_o Z_o$$

$$\Rightarrow \frac{V_o}{I_o} = \frac{Z_o}{1 + A\beta}$$

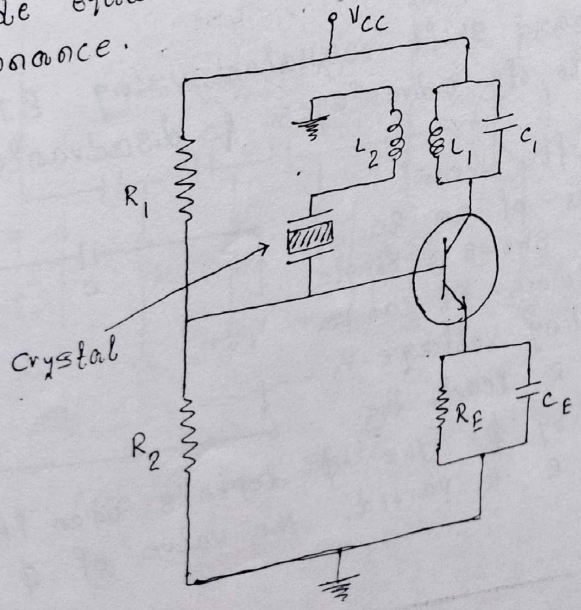
$$\Rightarrow \boxed{Z_{of} = \frac{Z_o}{1 + A\beta}} \longrightarrow (5)$$



(Equivalent circuit)

8. Explain the crystal oscinator with circuit diagram?

Sol^n:- A tank circuit ($L_1 C_1$) is placed in the collector & a crystal mounted between two plates is connected to the base of transistor. The coil L_1 is inductively coupled to L_2. The natural freⁿ of $L_1 C_1$ circuit is made equal to natural freⁿ of crystal to create resonance.



When the circuit is switched on it discharges through L_1. The oscillations produced later across L_1 are transferred to L_2 through transformer action. The positive feedback i.e. a phase difference of 180° is caused by transformer & further 180° by transistor action, thus the output is in phase with input which is fed to input of the transistor thus providing oscillations. A crystal oscillator can generate a freq between 5Hz to 25MHz with high reliability. Hence, the oscillator is frequently used in audio devices.

Advantages :-

→ It is very simple circuit as it doesn't need any tank circuit other than crystal itself.

→ Different oscillation freq can be had by simple replacing one crystal with another.

→ The Q-factor, which is measure of the quality of resonance circuit of a crystal is very high. The Q-factor of a crystal may range from 10^4 to 10^6 where as the LC circuit may have a Q-factor only the order of 100.

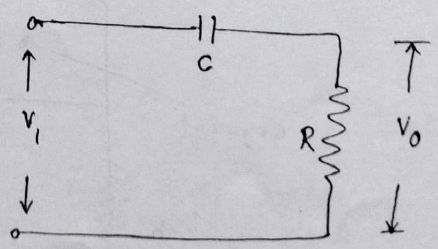
Disadvantages :-

→ The crystal oscillation have a very limited tuning range. They are used for freq exceeding 100KHz.

→ The crystal oscillator are fragile & therefore can only be used in low power circuits. //

9. Explain RC - Phase shift oscillator using BJT & OP-Amp & write its advantages & disadvantages ?

Sol^n :- A Phase shift circuit essentially consists of an RC-network. The fig. shows a single section of RC - network. It can be shown that alternating voltage V_0 appear across the R leads the applied voltage V_i by ϕ. The ϕ depends upon the value of R & C. If resistor R is varied, the value of ϕ is also varied.



If the voltage V_1 by 90° i.e. $\phi = 90°$, the output voltage V_o leads

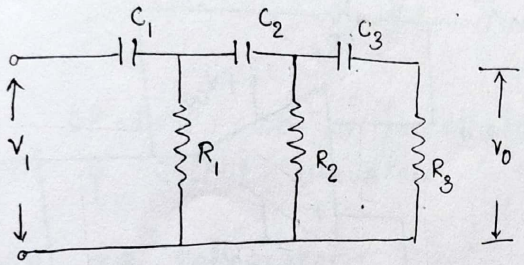
$$\phi = \tan^{-1}\frac{X_C}{R}$$

$$= \tan^{-1}\frac{1}{2\pi f RC}$$

When $R = 0$

$$\Rightarrow \phi = \tan^{-1}\infty = 90°$$

But practically $R \neq 0$, so for practical purpose we chose the value of R & C such that ϕ becomes 60°. So, we get 180° phase shift. So, we require three RC circuit is given below;

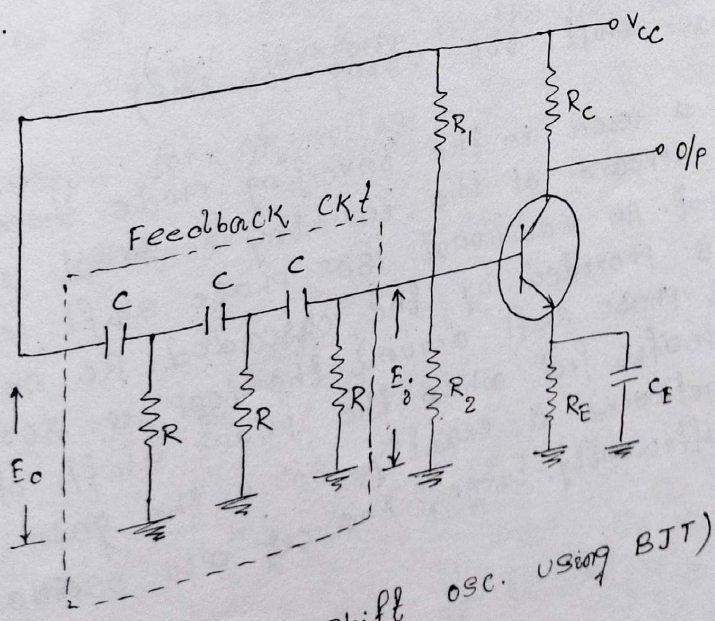


The freq of oscillation in RC phase-shift oscillator is given by,

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

where, $R_1 = R_2 = R_3 = R$

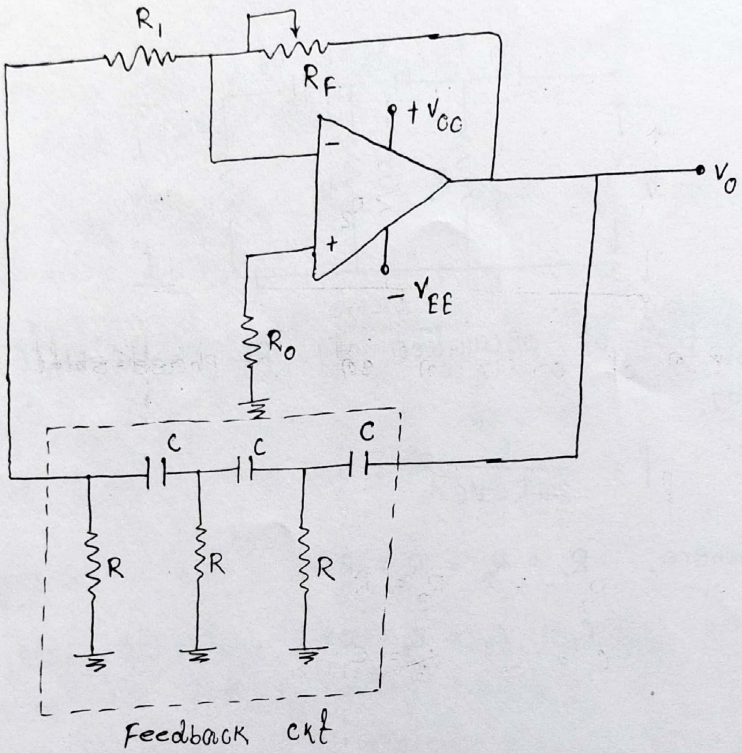
$C_1 = C_2 = C_3 = C$



(RC Phase shift osc. using BJT)

When the switch is ON, [illegible]
The o/p voltage E_o of the amplifier is feedback network. This network produces a phase shift of 180° & voltage E_i appear at its output which is applied to the transistor amplifier.

A phase shift of 180° is produced by transistor amplifier. A further phase shift of 180° is produced by the RC network. As a result, the phase shift of entire loop is 360°.



(RC Phase shift osc. using OP-Amp)

The OP-Amp is used in the inverting mode therefore any signal that appears at the inverting terminal is shifted by 180° at output. An additional 180° phase shift required for oscillation is provided by the cascaded RC networks. Thus the total phase shift around the loop is 360°. Now at the some specific freⁿ when the phase shift of the cascaded RC networks is exactly 180° & the gain of the amplifier is sufficiently large, the ckt will oscillate at that freⁿ.

Advantages :-

→ It is cheap & simple circuit as it contains resistors & capacitors.

→ It provides good freq stability.

→ The output is sinusoidal that is quite distortion free.

→ They have a wide freq range (few Hz to several 100 KHz)

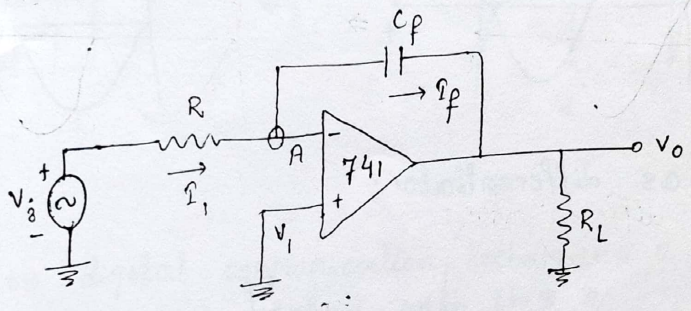
Disadvantages :-

→ The output is small. It is due to smaller feedback.

→ It is difficult for the ckt to start oscillation as the feedback is usually small. //

10. Explain OP-Amp as differentiator & integrator. Sketch the input & output waveform ?

Soln :- OP-Amp as Integrator ;



A circuit whose voltage at output is the integral of input voltage waveform is the integrator.

Expression for o/p voltage ;

Apply KCL at A,

$$I_1 - I_f = 0$$

$$\Rightarrow I_1 = I_f$$

$$\Rightarrow \frac{V_{in} - 0}{R} = C_f \frac{d}{dt}(V_c)$$

$$\Rightarrow \frac{V_{in}}{R} = C_f \frac{d}{dt}(0 - V_o)$$

$$\Rightarrow \frac{V_{in}}{R} = -C_f \frac{dV_o}{dt}$$

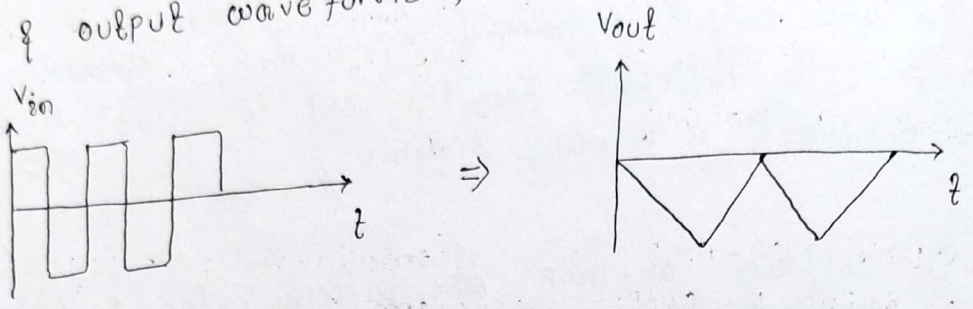
$$\Rightarrow \frac{dv_o}{dt} = -\frac{1}{RC_f} \cdot v_{in}$$

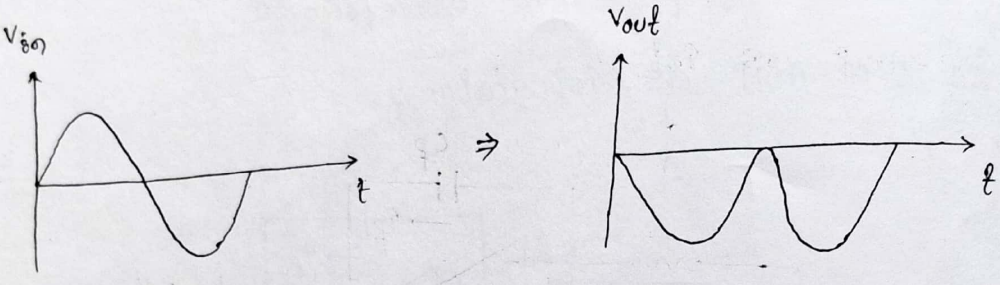
Integrating both sides w.r.t time,

$$\Rightarrow \int dv_o = -\int \frac{1}{RC_f} \cdot v_{in}\, dt$$

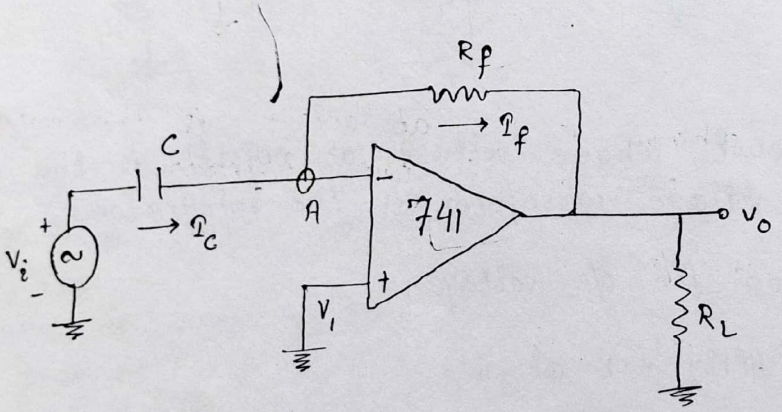
$$\Rightarrow v_o = -\frac{1}{RC_f} \int v_{in}\, dt$$

Input & output waveforms ;





OP-Amp as differentiator ;



The circuit in which the output waveform is the derivative of input waveform is called differentiator ckt.

Expression of o/p voltage ;

Apply KCL at A,

$$I_c - I_f = 0$$

$$\Rightarrow I_c = I_f$$

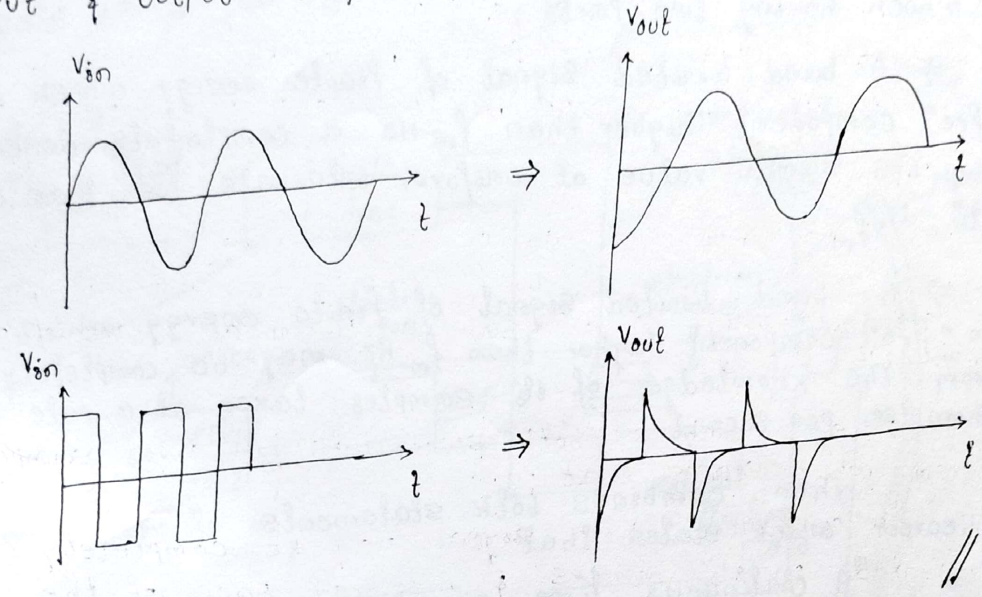
$$\Rightarrow C \cdot \frac{dV_c}{dt} = \frac{0 - V_o}{R_f}$$

$$\Rightarrow C \cdot \frac{d}{dt}(V_{in} - 0) = -\frac{V_o}{R_f}$$

$$\Rightarrow C \frac{dV_{in}}{dt} = -\frac{V_o}{R_f}$$

$$\Rightarrow V_o = -CR_f \frac{dV_{in}}{dt}.$$

Input & output waveforms;



11. What is digital communication techniques ? Explain the Sampling theorem related with this ?

Sol^n :-

Basics Digital communication Techniques ;

→ In a digital communication a base band digital information i.e. binary data is transmitted over bandpass communication channel.

→ The signals which are lies continous i.e. analog.

→ Hence these signals have to be converted into some digital form prior to actual transmission. This involves a process of Analog to Digital (A/D) conversion.

→ In the receiver the reverse process has to be facilated is Digital to Analog conversion (D/A) in order to obtain the base band signal.

→ For conversion of analog signal digital form we need three process i.e. sampling, Quantizaling & encoding.

Sampling :

→ sampling process is used to convert a continuous time signal into discrete time signal.

→ sampling process is based on the sampling theorem which having two parts :

⇒ A band limited signal of finite energy which has no freⁿ component higher than f_m Hz is completely described by its sample value at uniform intervals less than or equal to $1/2f_m$.

⇒ A band limited signal of finite energy which has no freⁿ component higher than f_m Hz may be completely received from the knowledge of its samples taken at a rate of $2f_m$ samples per second.

When combines both statements it gives sampling theorem which states that ;

"A continuous time signal may be completely represented in its samples & recovered back if the sampling freⁿ is $f_s \geq 2f_m$. Here, f_s is the sampling freⁿ & f_m is maxᵐ freⁿ present in the signal".

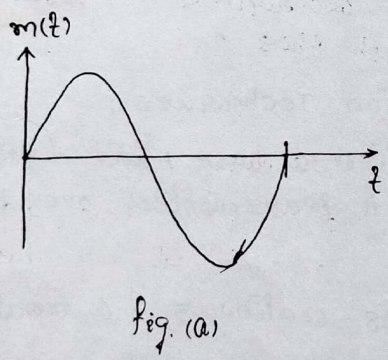


fig. (a)

A signal m(t) which is to be sampled.

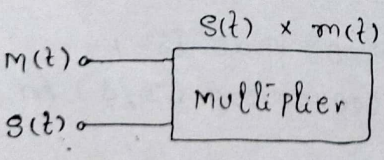


fig. (c)

The sampling oper is performed in a multiplier.

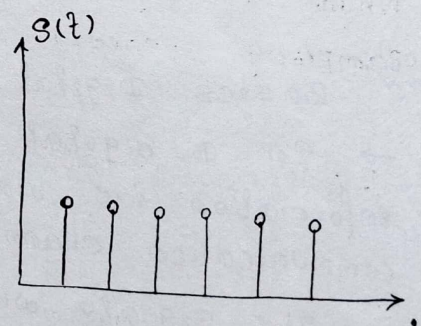


fig. (b)

The sampling freⁿ S(t) consists of train of very narrow amplitude.

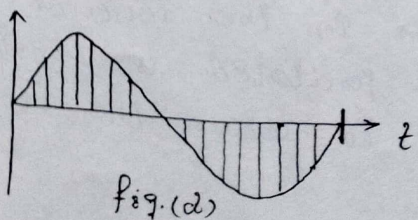


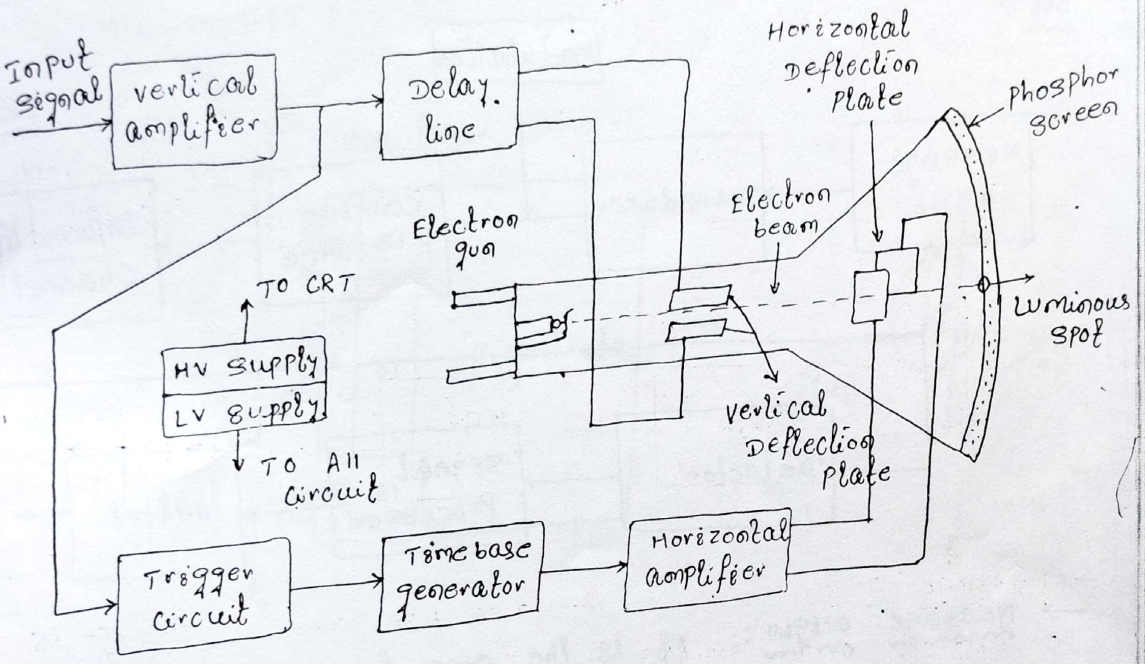
fig. (d)

The samples of the signal m(t).

Hence, in the sampling process sufficient no. of samples of the signals are taken so that the signal can be successfully recovered from these samples. //

12. Draw the functional block diagram of CRO ?

Sol?:- The CRO is an exteremely useful instrument used for studying wave shape of alternating currents & voltages as well as for measurement of voltage, current, power & freq. It allows the user to see the amplitude of electrical signals as a func? of time on the screen.



→CRT :- It is the heart of the CRO. It generates the electron beam, accelarates the beam to a high velocity, deflects the beam to create the image & contains a Phosphorous screen where the electron beams becomes visible.

→Power Supply :- It contains two voltages i.e. Low voltage supply which is required for the operation of different cut & generation of electron beam. High voltage supply of the order of few thousand is required for CRT to accelarate the beam.

→ Deflection plates :- It consists of Horizontal & vertical deflection plates which are fitted between electron gun & create a visible spot according to the input signal by deflecting the beam.

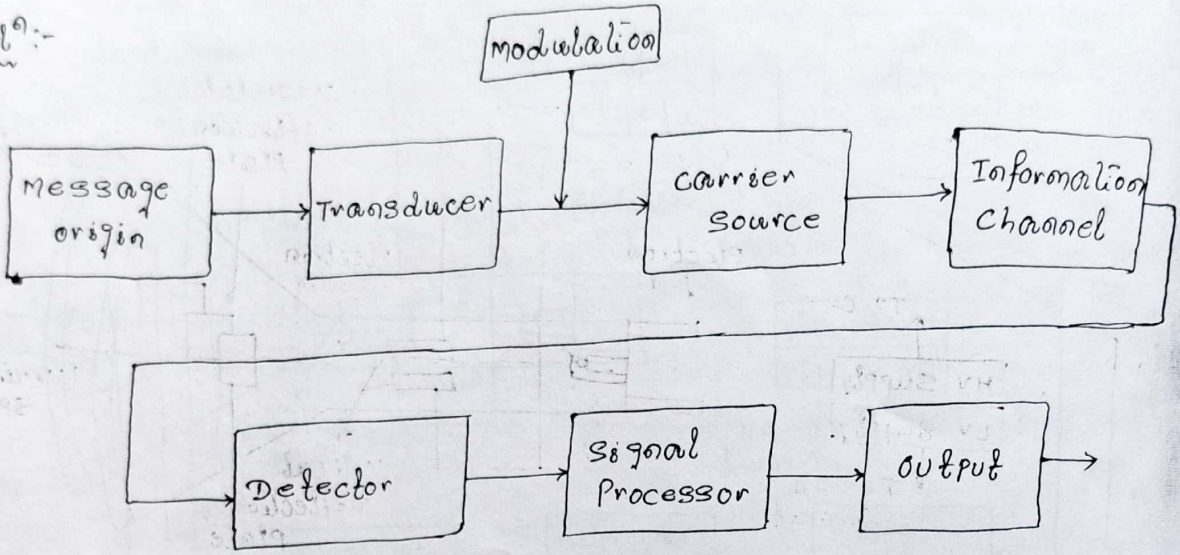
The signal which is to be measured is applied to vertical deflection plates & a sweep signal (saw tooth)

signal is applied to the horizontal deflection plate which deflects the spot with a constant time dependent rate on x-axis (horizontal).

→ Triggering circuit :- It is provided for synchronizing two types of deflection so that horizontal deflection spot starts at same point of the input vertical signal each time it sweeps. //

13. Explain the principle & operation of fibre optics communication system ?

Sol^{n} :-



→ Message origin :- It is the area from where message is originated or transmitted.

→ Transducer :- It is a device which converts a non-electrical quantity into electrical quantity.

→ Modulator :- Modulation is the process in which the characteristic of signal (amplitude, phase & freⁿ) varies according to the intensity of signal.

→ Carrier source :- The carrier source is responsible for carry the information from source to destination & also propagated to long distances.

→ Information channel :- It is the path through which the exchange of information takes place from source to destination.

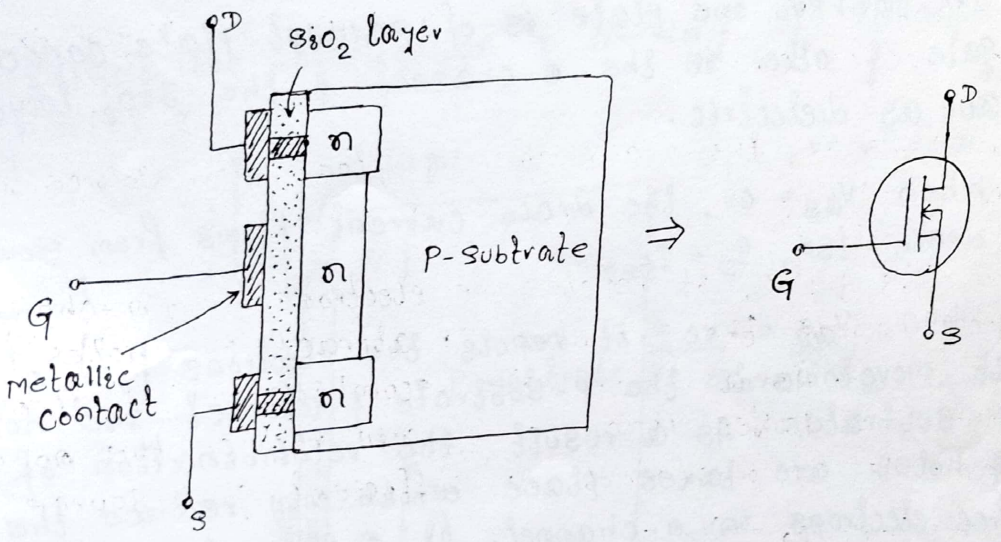
→ Detector :- It is also called demodulator, where the process of demodulation takes place i.e. here the information signal is separated from carrier.

→ Signal Processor :- Now the detected signal is filtered & amplified by the help of signal processor.

→ output :- Now the receiver recives the message output after it is processed. //

14. Explain the construction & working of N-channel DE-MOSFET ?

Sol^{n} :-



Construction :-

→ It consists of a conducting bar n-type material with an insulated gate on the left & P-substrate on the right.

→ Free electrons flow from source to drain through n-channel

→ A thin layer of SiO_2 is deposited on the left of the n-channel which revels that;

(i) it increases the input impedance of MOSFET.

(ii) there is no direct contact between the gate & channel.

(iii) due to this, a negligible gate current flows from source to drain when V_{GS} is +ve..

Operation :-

→ There are two types of operations ;

(i) Depletion - type MOSFET , when V_{GS} is -ve.

(ii) Enhancement - type MOSFET, when V_{GS} is +ve.

→ Since D - MOSFET can operate in two modes i.e. depletion as well as enhancement . So, it is called DE - MOSFET.

→ The Principle of working of D - MOSFET is based on the working of Parallel plate capacitor . If one plate of capacitor is +ve it induce a -ve charge on the opposite plate & viceversa.

→ In MOSFET, one plate of parallel plate capacitor is gate & other is the n-channel & the SiO_2 layer is act as dielectric.

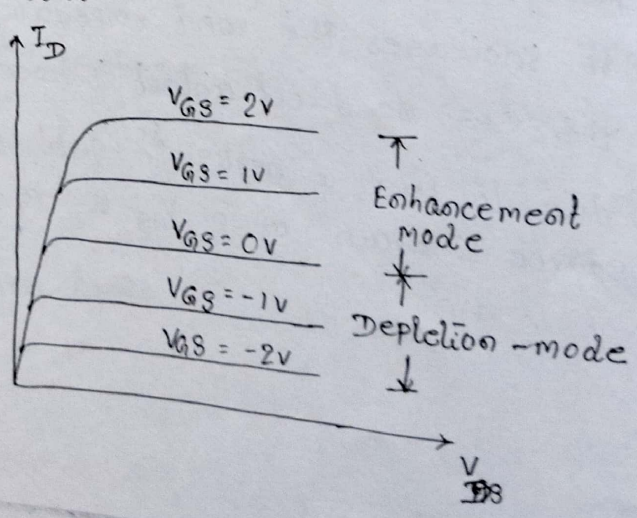
→ When $V_{GS} = 0V$, the drain current flows from Source to drain . So, $I_D = I_{DSS}$.

→ When V_{GS} = -ve, it repels the electrons from n-channel to move towards the P-substrate & attract the holes from P-substrate . As a result, the recombination of electrons & holes are takes place which will reduce the no. of free electrons in n-channel. At sufficient gate-source voltage $V_{GS(off)} = V_P$.

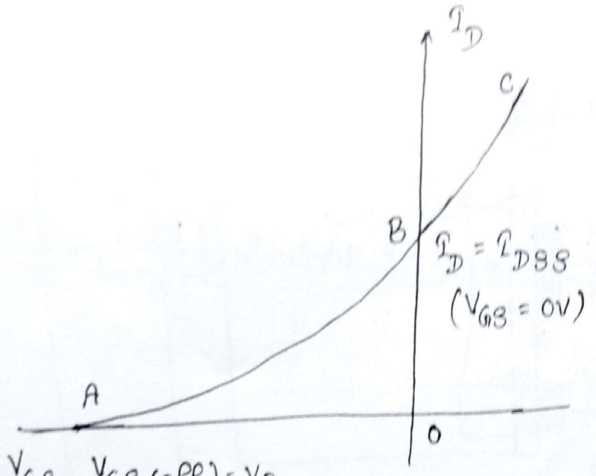
→ When V_{GS} = +ve, the +ve gate will draw additional free electrons from P-substrate . As V_{GS} will continuously increase , I_D will increase in rapid rate.

Characteristics :-

⇒ Drain characteristics :-



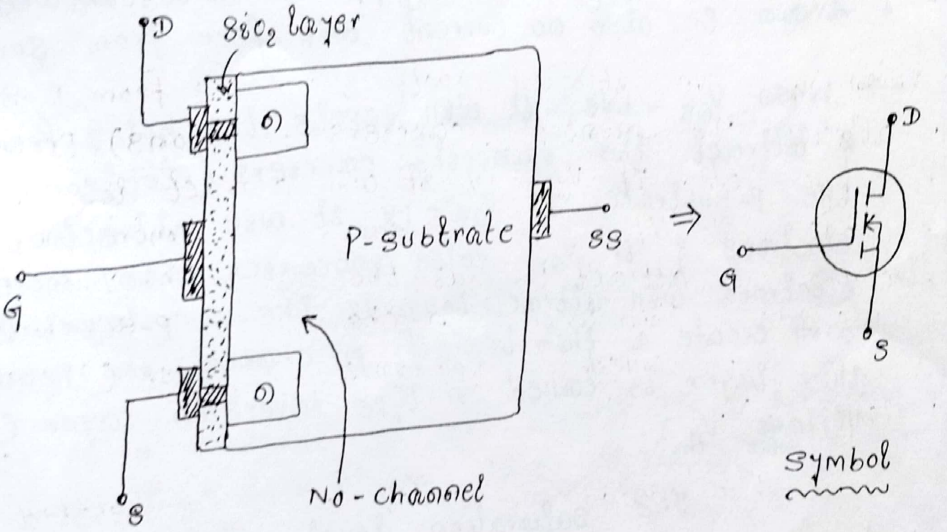
⇒ Transfer characteristics :-



//

15. Explain the construction & working of Enhancement-MOSFET ?

Sol^n :-



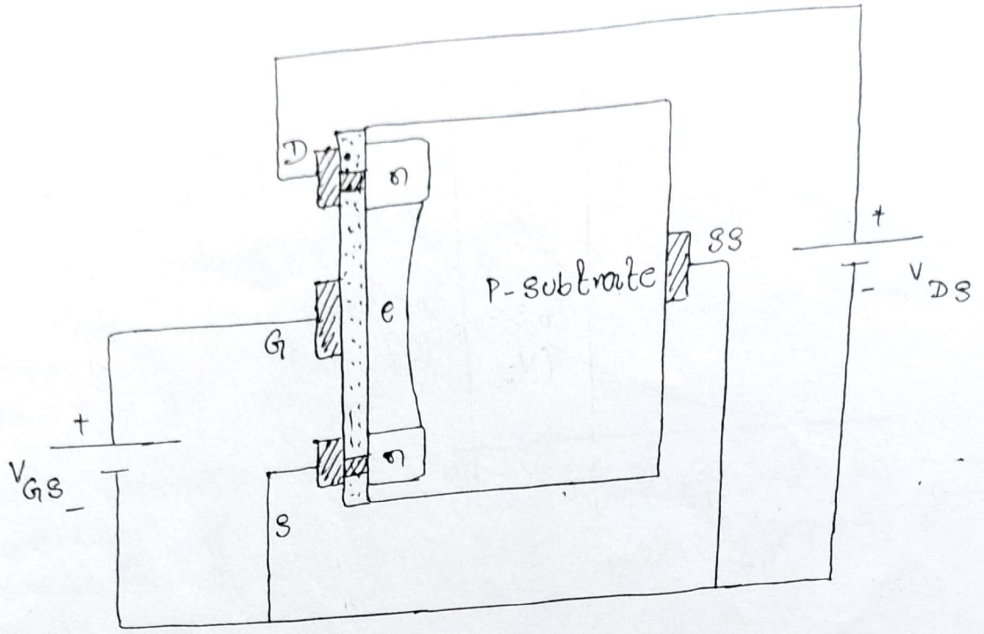
Constructions :-

→ The E-MOSFET has no depletion mode & it operates in enhancement mode.

→ The primary difference between D-MOSFET & E-MOSFET is there is absence of channel in between drain & source.

Operations :-

→ When $V_{GS} = 0V$, $I_D = 0mA$ & no current will flow from source to drain, as there is no-channel between source to drain.



→ when V_{GS} = -ve, it will attracts the holes from P-substrate & create a layer of holes between source & drain. so, also no current will flow from source to drain.

→ when V_{GS} = +ve, it will repels the holes from P-substrate & attract the minority carriers (electrons) present in the P-substrate. If V_{GS} = 1V, it will attract less amount of electrons & if V_{GS} value increases than more no. of electrons will attract towards the SiO_2 layer. This effect will create a thin layer of n-channel in P-substrate & this layer is called n-type inversion layer (threshold voltage V_{th}).

The saturation level of V_{DS} is related to V_{GS} by,

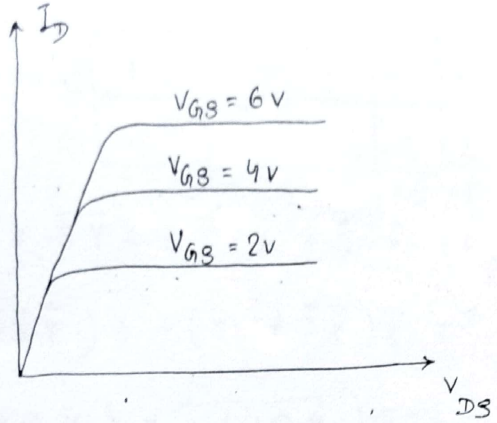
$$V_{DS(sat)} = V_{GS} - V_{th}$$

For $V_{GS} < V_{th}$, $I_D = 0$ mA

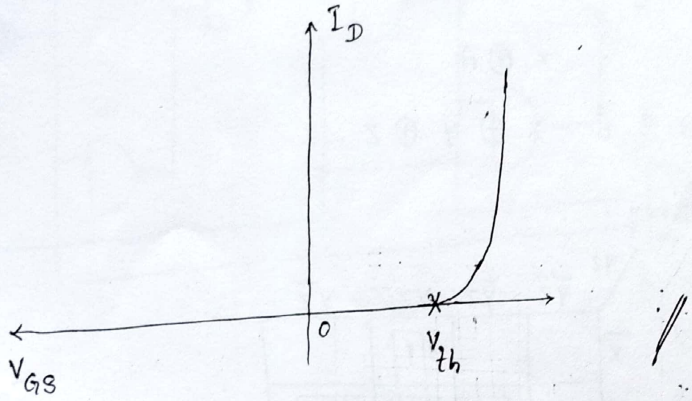
$V_{GS} > V_{th}$, $I_D = K (V_{GS} - V_{th})^2$

where, K = constant.

→ Drain characteristics :-

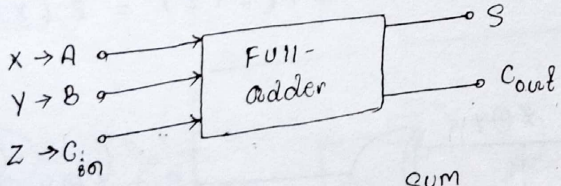


→ Transfer characteristics :-



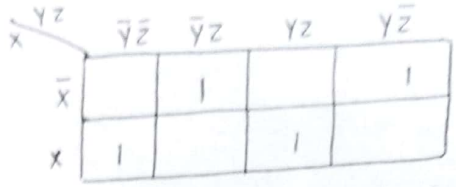
16. Explain Full adder using logic diagram & Realise it using NAND & NOR gates ?

Sol^n :- It is a combinational logic circuit that performs the addition of 3 binary bits. The result produce sum & carry.



Inputs			Sum	carry
A(x)	B(Y)	C_{in}(Z)	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

For sum ;



So, $S = \bar{x}\bar{y}\bar{z} + \bar{x}y\bar{z} + x\bar{y}\bar{z} + xyz$

$= \bar{x}(\bar{y}\bar{z} + y\bar{z}) + x(\bar{y}\bar{z} + yz)$

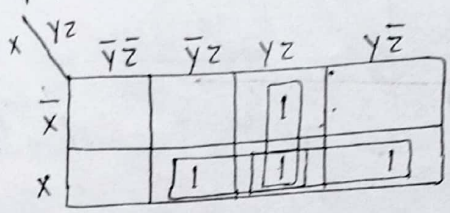
$= \bar{x}(y \oplus z) + x(y \odot z)$

$= \bar{x}A + x\bar{A} \quad (\because A = y \oplus z)$

$= x \oplus A$

$\Rightarrow S = x \oplus y \oplus z.$

For carry ;

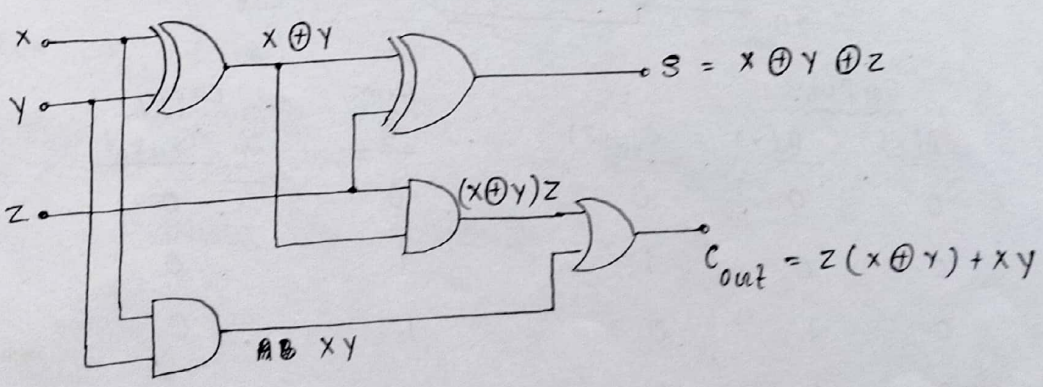


So, $C_0 = \bar{x}y\bar{z} + x\bar{y}z + xy\bar{z} + xyz$

$= x(\bar{y}z + y\bar{z}) + yz(\bar{x} + x)$

$= x(y \oplus z) + yz$

$= z(x \oplus y) + xy(z + \bar{z}) = z(x \oplus y) + xy$



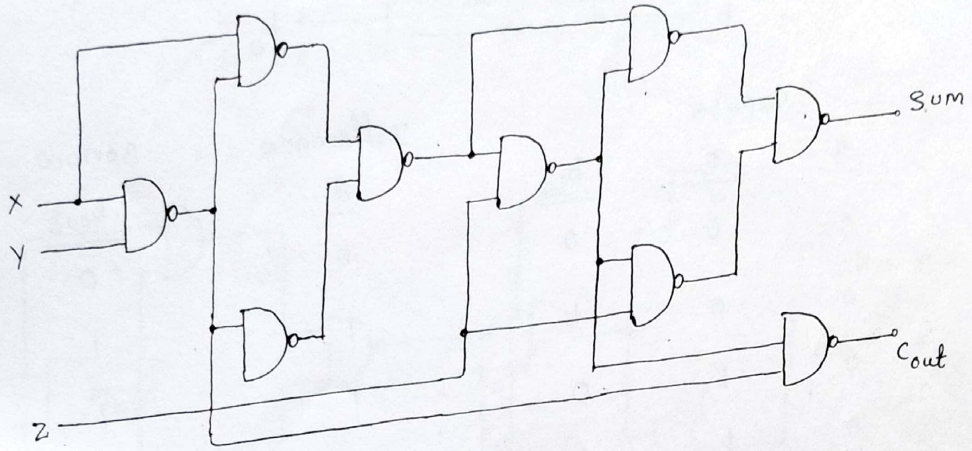
(Logic - Diagram)

Full - Adder using NAND logic :-

$$X \oplus Y = \overline{X \cdot \overline{XY}} \cdot \overline{Y \cdot \overline{XY}} = P$$

Now, $S = X \oplus Y \oplus Z = \overline{P \cdot \overline{PZ}} \cdot \overline{Z \cdot \overline{PZ}}$

& $C_0 = Z(X \oplus Y) + XY = \overline{Z(X \oplus Y) \cdot \overline{XY}}$

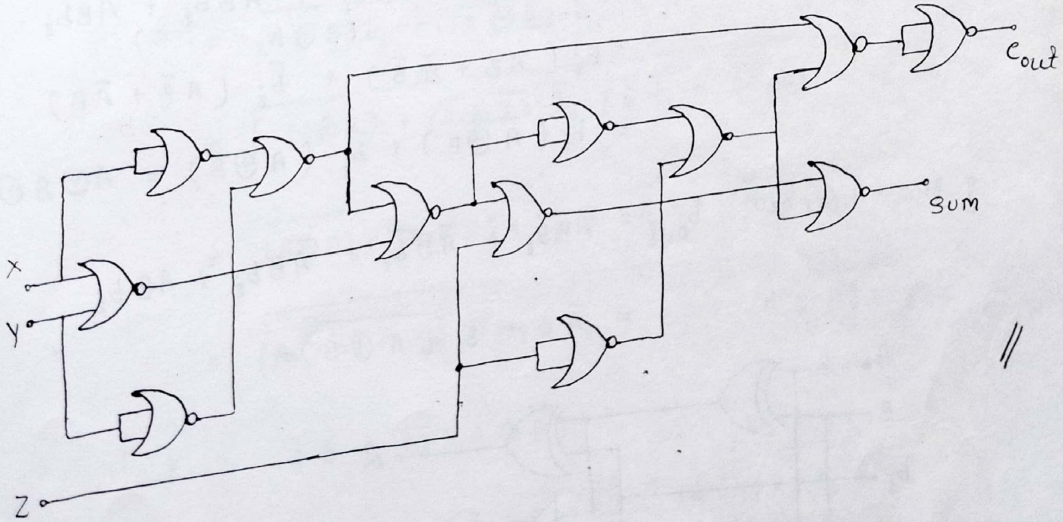


Full - Adder using NOR logic :-

$$X \oplus Y = P = \overline{\overline{(A+B)} + \overline{A} + \overline{B}} = \overline{\overline{(X+Y)} + \overline{X} + \overline{Y}}$$

Now, $S = X \oplus Y \oplus Z = P \oplus Z = \overline{\overline{P+Z} + \overline{P+\overline{Z}}}$

& $C_{out} = XY + Z(X \oplus Y) = \overline{\overline{X} + \overline{Y}} + \overline{\overline{Z} + X \oplus Y}$



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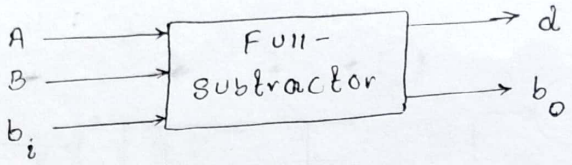
17. Explain Full-subtractor using logic diagram & Realise it using NAND & NOR logic ?

Soln:- It is a combinational logic circuit that performs subtraction of three bits & provide two outputs difference & borrow.



Inputs			Difference	Borrow
A	B	b_{in}	d	b_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1.

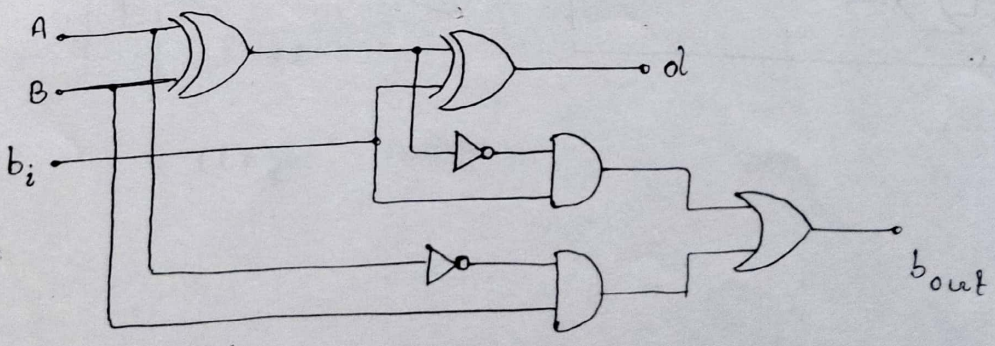
The difference, $d = \bar{A}\bar{B}b_i + \bar{A}B\bar{b}_i + A\bar{B}\bar{b}_i + ABb_i$

$= b_i(AB + \bar{A}\bar{B}) + \bar{b}_i(A\bar{B} + \bar{A}B)$

$= b_i(\overline{A \oplus B}) + \bar{b}_i(A \oplus B) = A \oplus B \oplus b_i$

& the borrow; $b_{out} = \bar{A}\bar{B}b_i + \bar{A}B\bar{b}_i + \bar{A}Bb_i + ABb_i$

$= \bar{A}B + b_i\overline{(A \oplus B)}$.



(Logic - Diagram)

Full - Subtractor using NAND logic ;

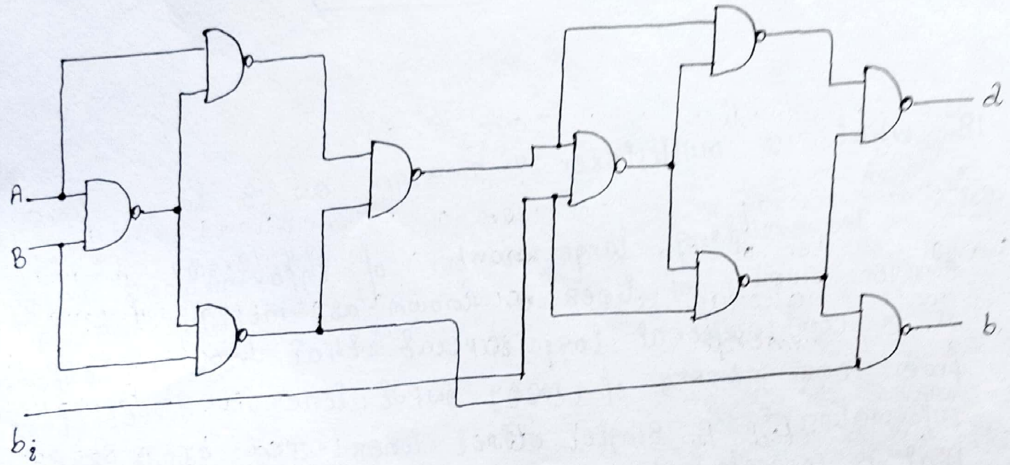
$$d = A \oplus B \oplus b_i = \overline{(A \oplus B)\,\overline{(A \oplus B)}\,b_i} \cdot \overline{b_i\,\overline{(A \oplus B)}\,b_i}$$

$$b_{out} = \bar{A}B + b_i\,(A \oplus B)$$

$$= \overline{\overline{\bar{A}\,B} + \overline{b_i\,(A \oplus B)}} = \overline{\bar{A}\,B} \cdot \overline{b_i\,(A \oplus B)}$$

$$= \overline{B\,(\bar{A} + \bar{B}) \cdot b_i\,[\,\bar{b}_i + (A \oplus B)\,]}$$

$$= \overline{B \cdot \overline{AB} \cdot b_i\,[\,\overline{b_i \cdot (A \oplus B)}\,]}$$



Full - Subtractor using NOR logic ;

$$d = A \oplus B \oplus b_i$$

$$= \overline{(A \oplus B)\,b_i + \overline{(A \oplus B)}\,\bar{b}_i}$$

$$= \overline{[\,(A \oplus B) + \overline{(A \oplus B)} \cdot \bar{b}_i\,]\,[\,b_i + \overline{(A \oplus B)}\,\bar{b}_i\,]}$$

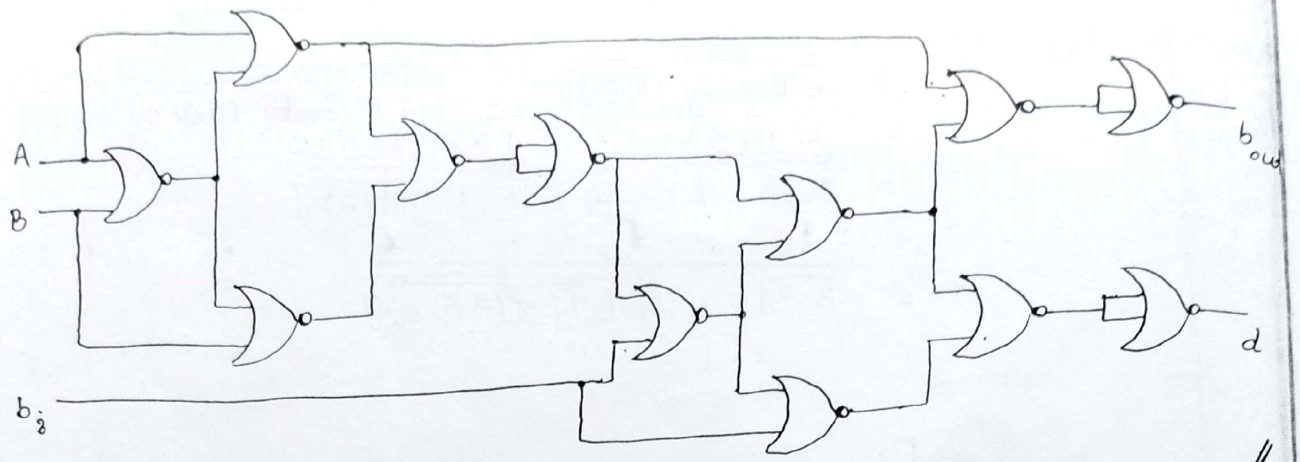
$$= \overline{(A \oplus B) + \overline{(A \oplus B)} + b_i} + \overline{b_i + \overline{(A \oplus B)} + b_i}$$

$$= \overline{\overline{(A \oplus B) + \overline{(A \oplus B)} + b_i} + b_i + \overline{(A \oplus B) + b_i}}$$

$$b_{out} = \bar{A}\,B + b_i\,\overline{(A \oplus B)}$$

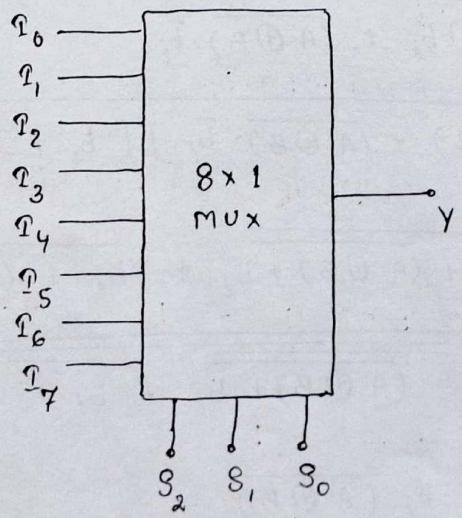
$$= \bar{A}\,(A + B) + \overline{(A \oplus B)}\,[\,(A \oplus B) + b_i\,]$$

$$= \overline{\overline{A + \overline{(A + B)}} + \overline{(A \oplus B) + [(A \oplus B) + b_i]}} \cdot$$



18. What is multiplexer ? Design an 8 to 1 line mux. ?

Sol^n:- Transmitting large number of informations using smaller number of lines is known as multiplexing. A mux is a combinational logic circuit that receives information from one of many input lines & direct these information to a single output lines. The input information that is connected to output line is controlled by a set of selection lines. A multiplexer with 2^n inputs require 'n' selection lines. It is also known as many to one data selector.

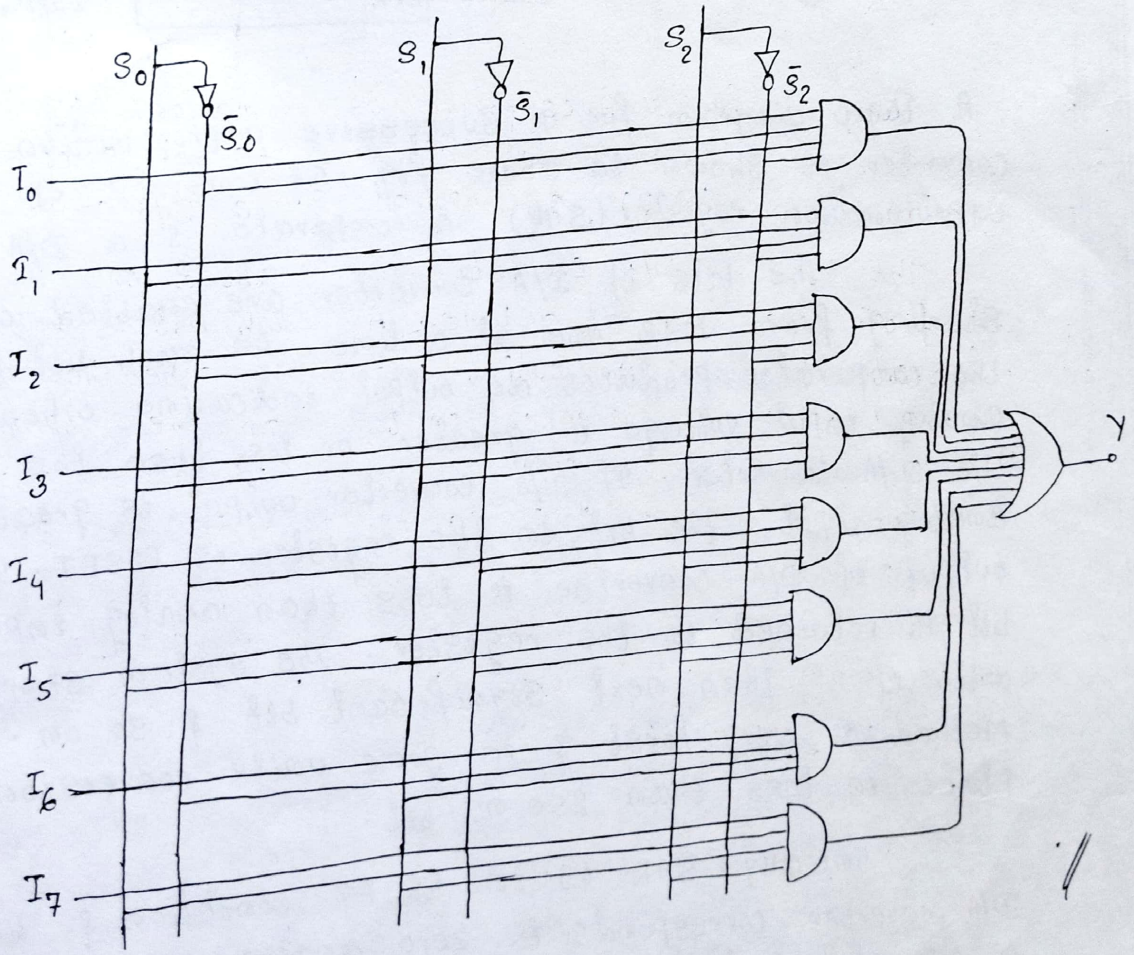


Function Table

S_2	S_1	S_0	y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

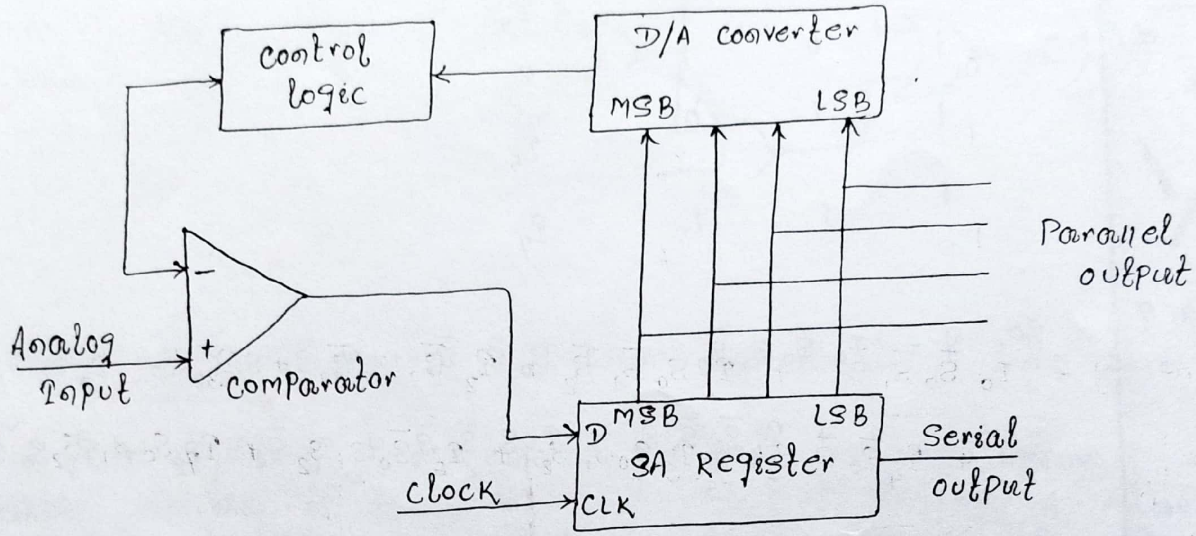
So, $y = I_0 \bar{S}_0 \bar{S}_1 \bar{S}_2 + I_1 S_0 \bar{S}_1 \bar{S}_2 + I_2 \bar{S}_0 S_1 \bar{S}_2 + I_3 S_0 S_1 \bar{S}_2$

$+ I_4 \bar{S}_0 \bar{S}_1 S_2 + I_5 S_0 \bar{S}_1 S_2 + I_6 \bar{S}_0 S_1 S_2 + I_7 S_0 S_1 S_2$



19. Explain the working of A/D conversion ?

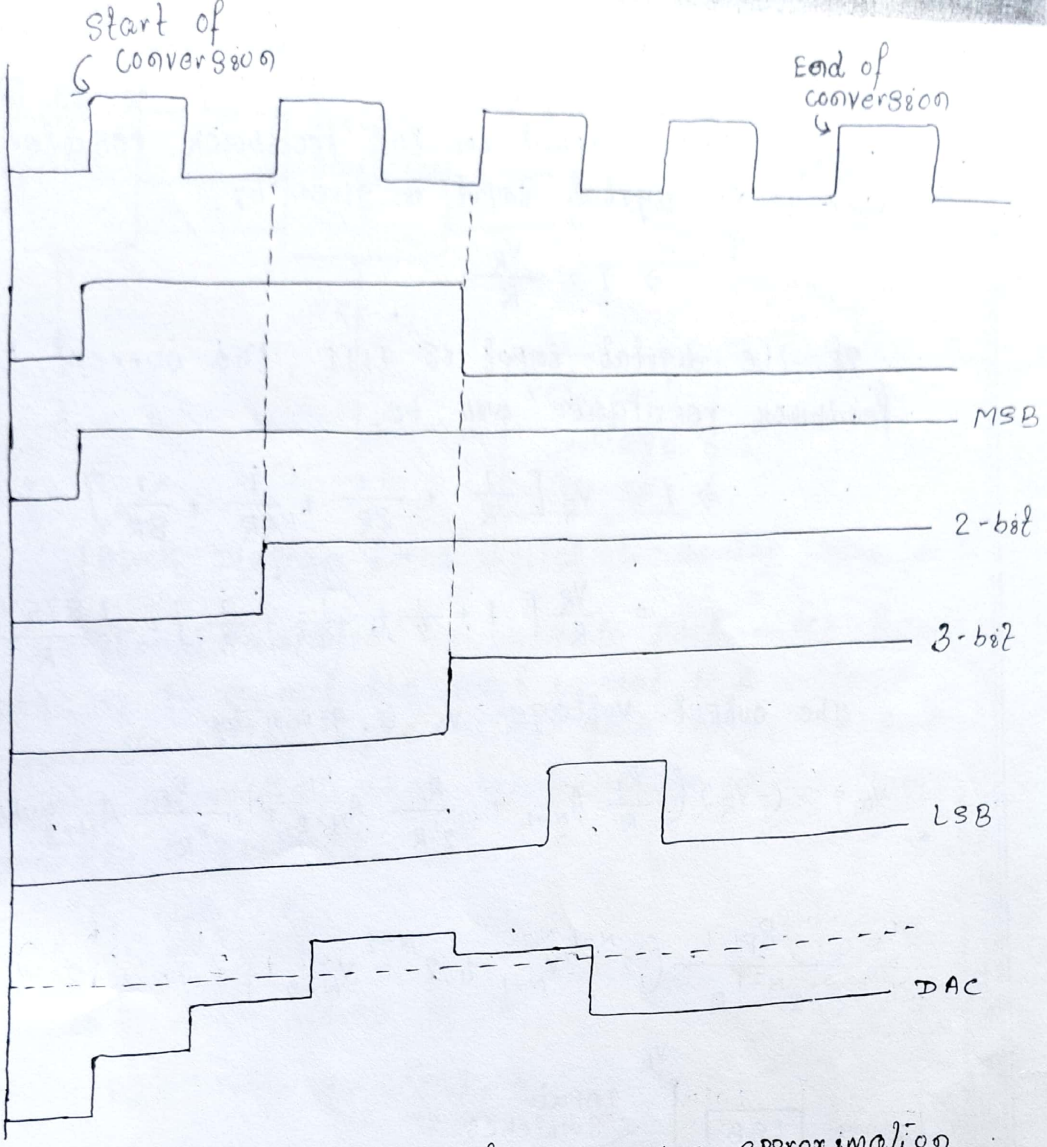
Soln:- Most of the information is processed by computer in analog form. So, it first convert into digital form. This process of converting analog voltages into an equivalent digital signal is known as analog to digital conversion & the device which performs this is called analog to digital converter or A/D converter.



A logic diagram for a successive approximation A/D converter is shown in above fig. It consists of successive approximation register (SAR), a comparator & a D/A converter.

The bits of D/A converter are enabled one by one starting from MSB one at a time. As each bit is enabled, the comparator produces an output indicating wheather the analog input voltage is greater or less than the output of the D/A converter. If D/A converter output is greater than analog input, the bit in the register is RESET. If the output of D/A converter is less than analog input, the bit is retained in the register. The system starts this with MSB, then next significant bit & so on. This method is very first & in some units conversion takes place in less than 250 ns/bit.

Initially SAR is in RESET condition & the o/p of D/A converter corresponds to zero analog input. On receiving a convert signal the system enters sequentially (starting from MSB) each bit input to the D/A converter to determine the relative weightage in comparison to the input.



(Timing Diagram of successive approximation of DAC). //

20. Explain the working of D/A conversion ?

Soln:- A digital signal can converted into analog signal, when each bit in the weighted code manner. A digital to analog conversion (D/A) is an important interface process for I/O operations.

A basic 4-bit resistor D/A converter is shown in fig. The resistances used has the values that represent the binary weights of the input bits of the digital code. The op-Amp offers a very high impedance to load to the resister network, & its inverting input looks like virtual ground. As a result the current through feedback resistance is sum of input currents & the output is proportional to the current through the R_F. The inverting input to the op-Amp is at 0V.

The resistors are multiples of R i.e. 2R, 4R, 8R corresponds to the binary weights 2^2, 2^1, 2^0. If V_R is the reference voltage, then current in the feedback resistor when a state 1000 is at digital input is given by,

$$\Rightarrow I = \frac{V_R}{R}$$

If the digital input is 1111, the current through the feedback resistance will be,

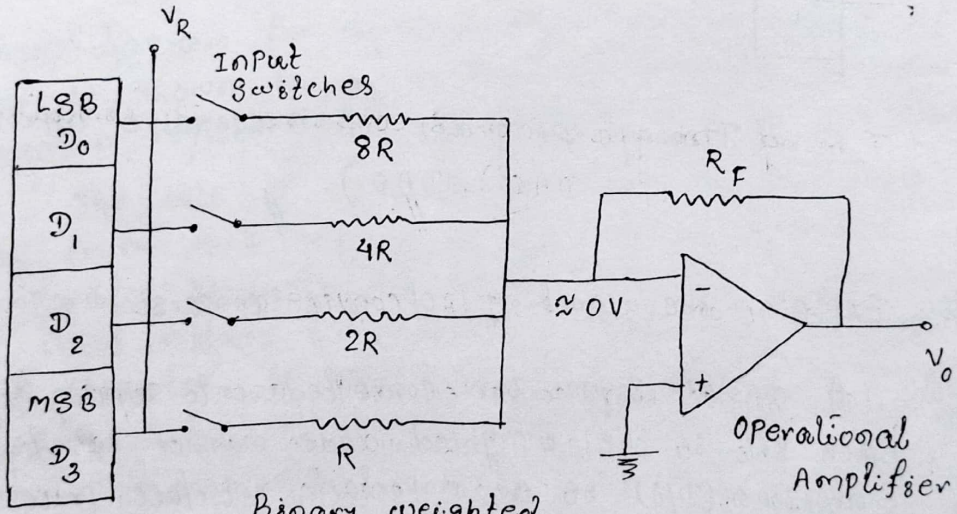
$$\Rightarrow I = V_R \left[\frac{1}{R} + \frac{1}{2R} + \frac{1}{4R} + \frac{1}{8R} \right]$$

$$= \frac{V_R}{R} \left[1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8} \right] = \frac{1.875 V_R}{R}$$

The output voltage V_o is given by,

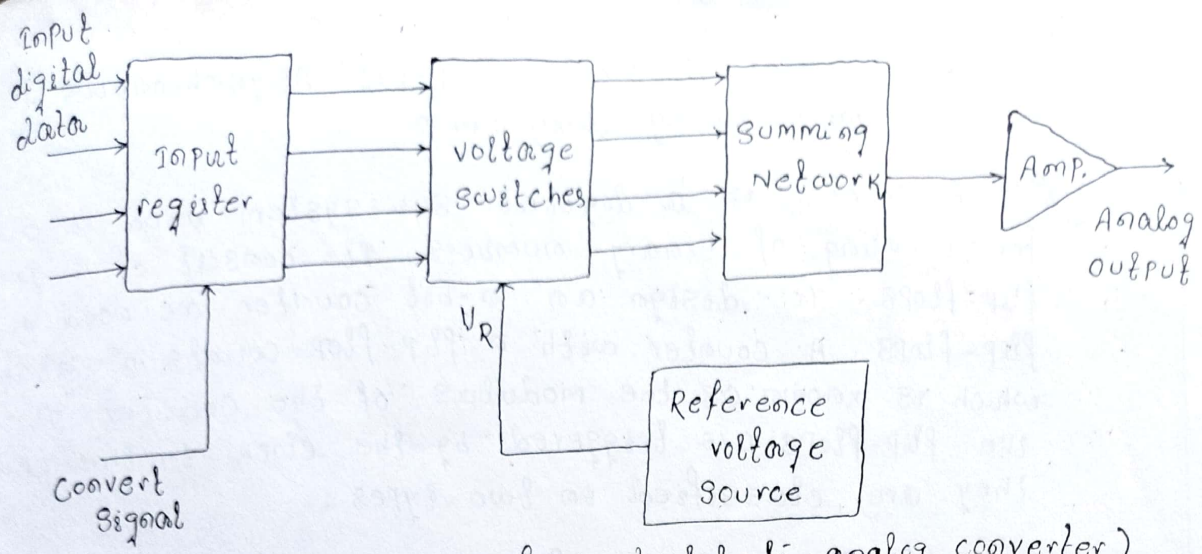
$$V_o = -(-V_R) \left(\frac{R_F}{R} A_{N-1} + \frac{R_F}{2^1 R} A_{N-2} + \frac{R_F}{2^2 R} A_{N-3} + \cdots + \frac{R_F}{2^{N-1} R} A_0 \right)$$

$$= \frac{R_F}{2^{N-1} R} \left(2^{N-1} V_{N-1} + 2^{N-2} V_{N-2} + \cdots + 2^1 V_1 + 2^0 V_0 \right)$$



Binary weighted resistors.

The below fig. shows the block diagram of digital to analog converter. The input register is a parallel in-parallel out device & has a convert signal. When a convert signal is high, the binary data is clocked into the register where it is stored until a next convert signal is received. The voltage switches are integrated circuits containing a field effect transistor & they connect or disconnect giving V_R.



(Block Diagram for a digital-to-analog converter)

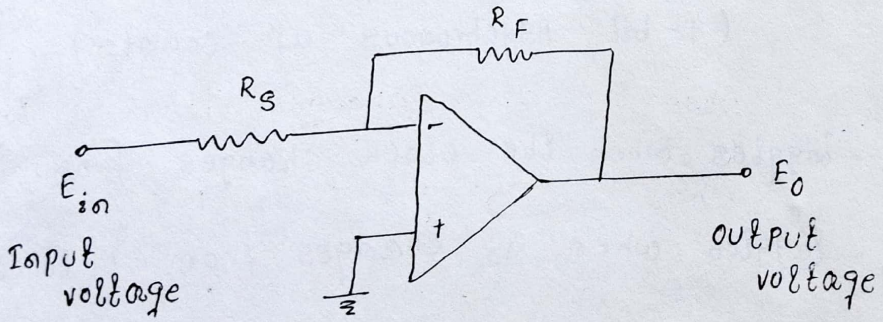
The operational amplifier is used to perform the following operations; (i) to convert the input current to a voltage (ii) to scale the voltage. The voltage gain of an op-Amp is shown in below fig, when input voltage is E_{in} through resistance R_S is given by,

$$I = \frac{E_{in}}{R_S}$$

The voltage drop across R_F is;

$$E_0 = IR_F = \left(-\frac{E_{in}}{R_S}\right) \times R_F$$

The -ve sign indicates that the current through resistor R_F is in the opposite direction from the current through R_S.



The voltage gain, $A_V = \frac{E_0}{E_{in}} = \left(-\frac{E_{in}}{R_S}\right) \times R_F \times \frac{1}{E_{in}}$

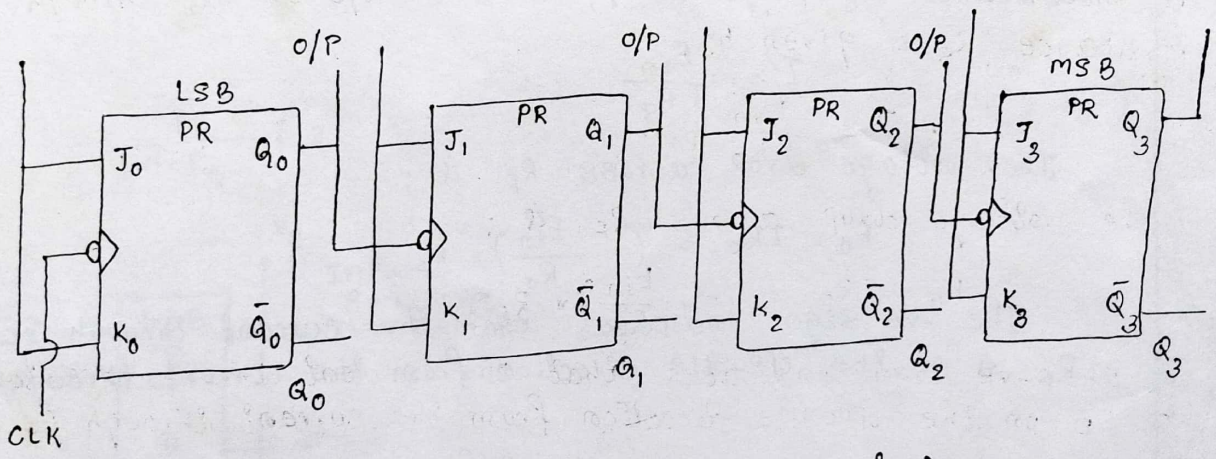
$$\Rightarrow A_V = -\frac{R_F}{R_S}$$

21. What is counter ? Explain 4-bit Asynchronous up counter with timing diagram ?

Sol^{n} :- A counter is a digital sub-system used in computer for counting of binary numbers. It consist of a group of flip-flops. To design an n-bit counter we need n flip-flops. A counter with n flip-flop counts 2^n states which is known as the modulus of the counter. The way the flip-flops are triggered by the clock in the counter, they are classified in two types :

1. Asynchronous counter.
2. Synchronous counter.

Depending on the counting sequence, counters are classified into various types ; up counter, down counter & up-down counter.



(4-bit Asychronous up counter)

(i) Q_0 - toggles when the clock changes from 1 to 0.

(ii) Q_1 - toggles when Q_0 changes from 1 to 0.

(iii) Q_2 - toggles when Q_1 changes from 1 to 0.

(iv) Q_3 - toggles when Q_2 changes from 1 to 0.

In this counter the flip-flops are triggered by the normal output of the previous flip-flops.

clock pulse	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Timing - Diagram ;